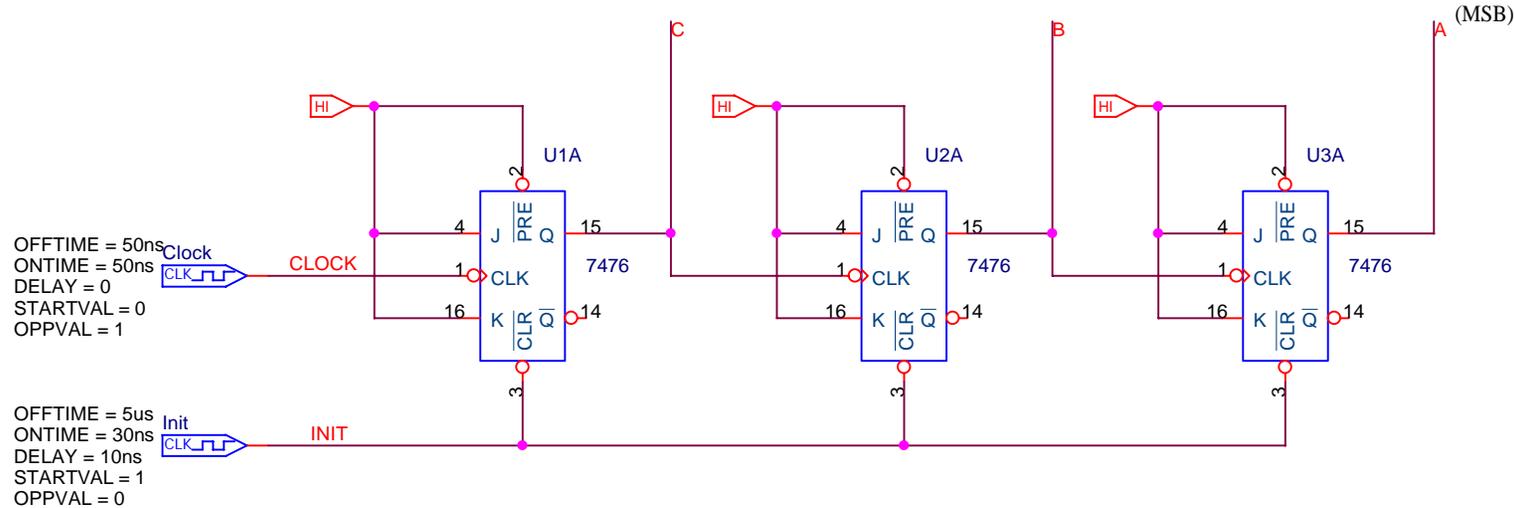


3-Bit Ripple Counter

Purpose: Ripple counters can be simple to design, but may have problems with propagation delay when clocked at high frequencies. The counter below is clocked at 10 MHz and several incorrect counts are apparent in the output timing diagram (first graph).

Analysis: A TRANSIENT analysis is performed in order to show the output for 10 counts. Since the clock has a period of 100ns, the transient analysis is performed for (10 counts)(100 ns/count) = 1us.

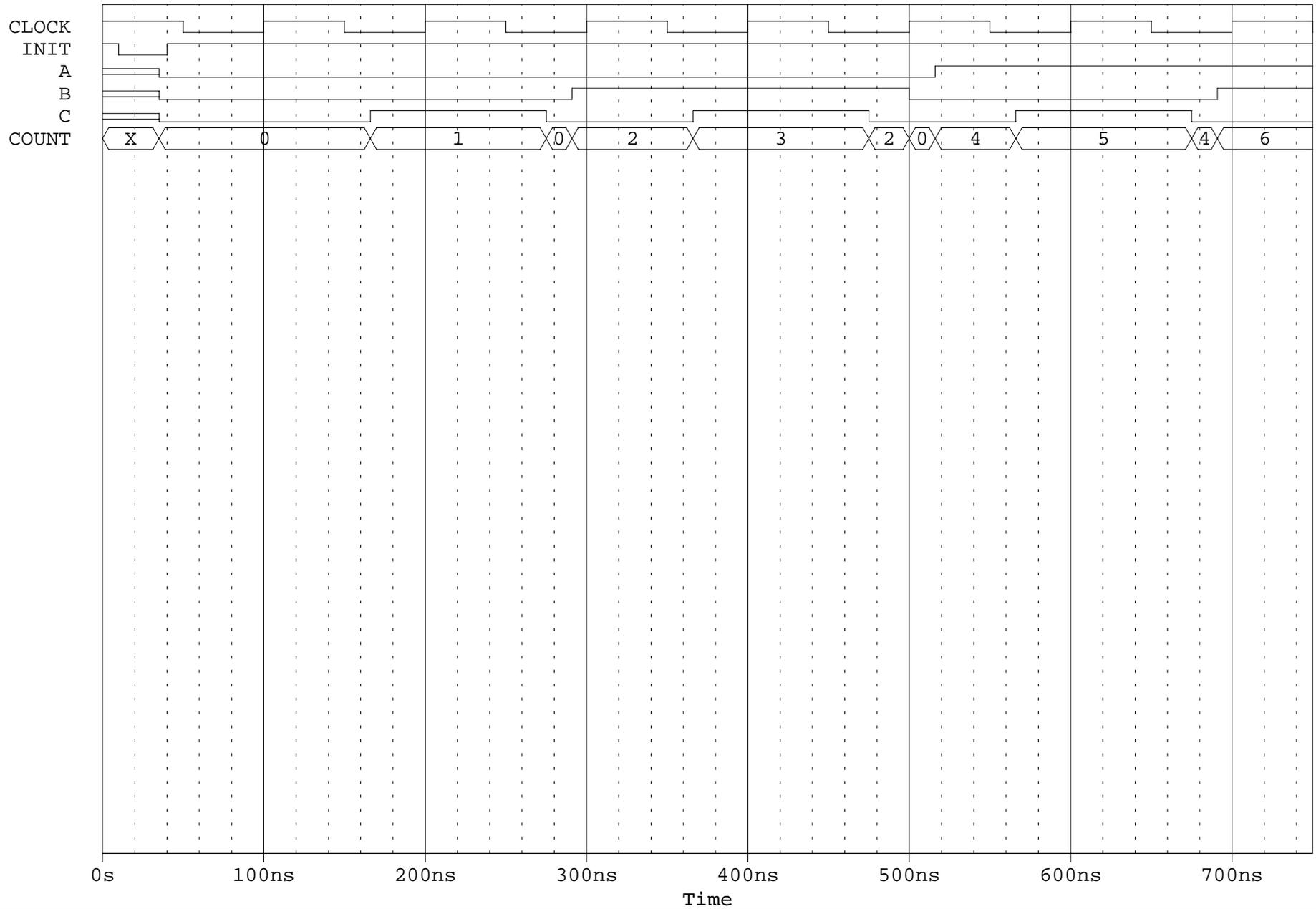


Notes:

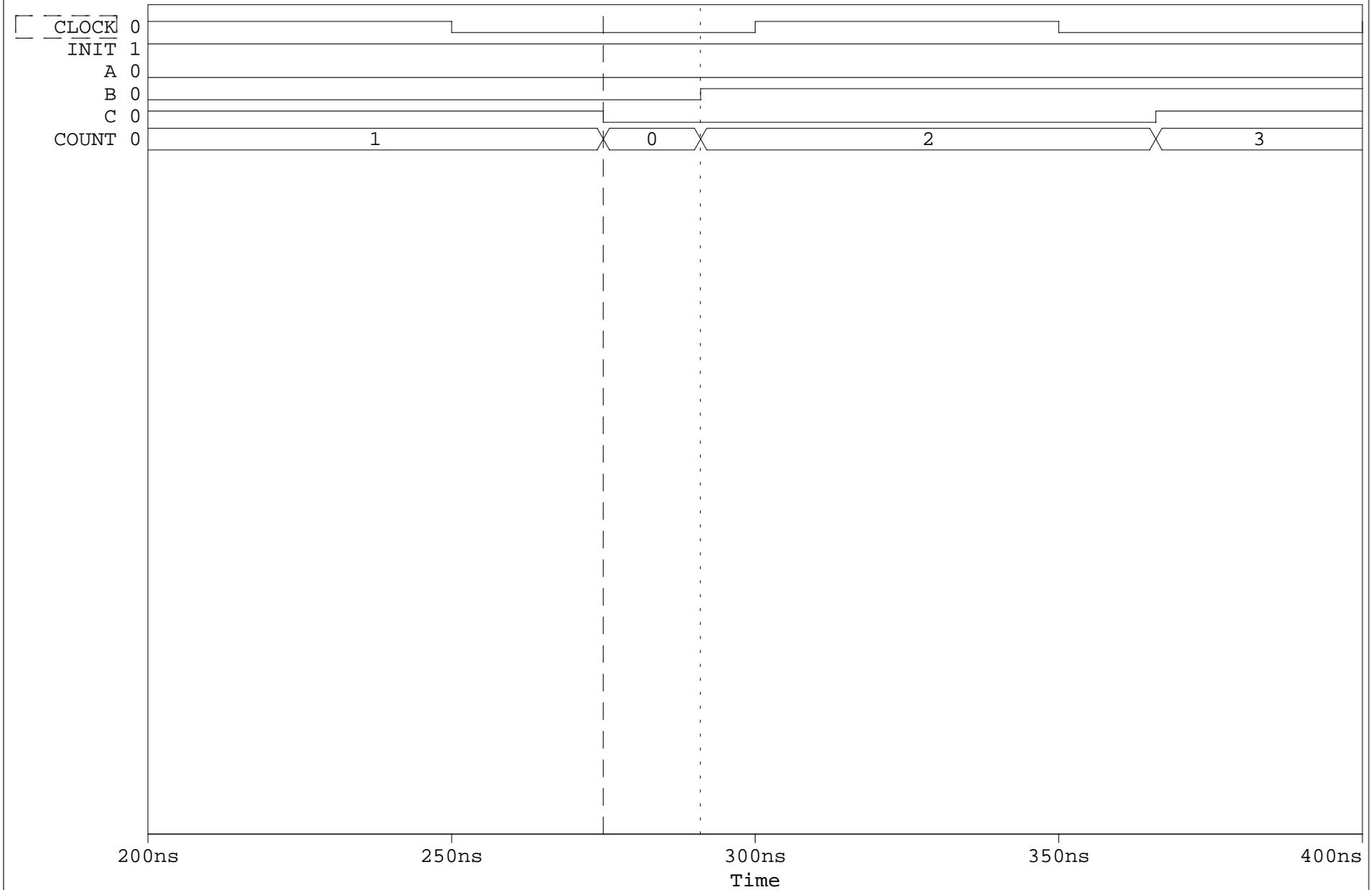
- 1) Analysis of this circuit may yield several "Digital Simulation Warnings" due to propagation delay problems. However, the analysis will still be completed.
- 2) PSPICE uses typical propagation delay values of $T_{phl} = 25$ ns and $T_{plh} = 16$ ns (see second and third graphs).
- 3) The part \$D_HI is used to apply a logical HI to the circuit. This part is found by selecting the GND icon on the toolbar.
- 4) Key wires were labeled A, B, C, INIT, and CLOCK so that they can be easily identified on the graphs. Labels are added by selecting the wire and then using the N1 icon on the toolbar.
- 5) The ONTIME for INIT was set to 30ns. A smaller ONTIME (25ns or less) will yield undefined outputs since the propagation delay for the gate is $T_{phl} = 25$ ns and thus the gate needs at least 25ns to be cleared (I discovered this the hard way).

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(A) Note that several counts in this 3-bit counter are incorrect due to propagation delay

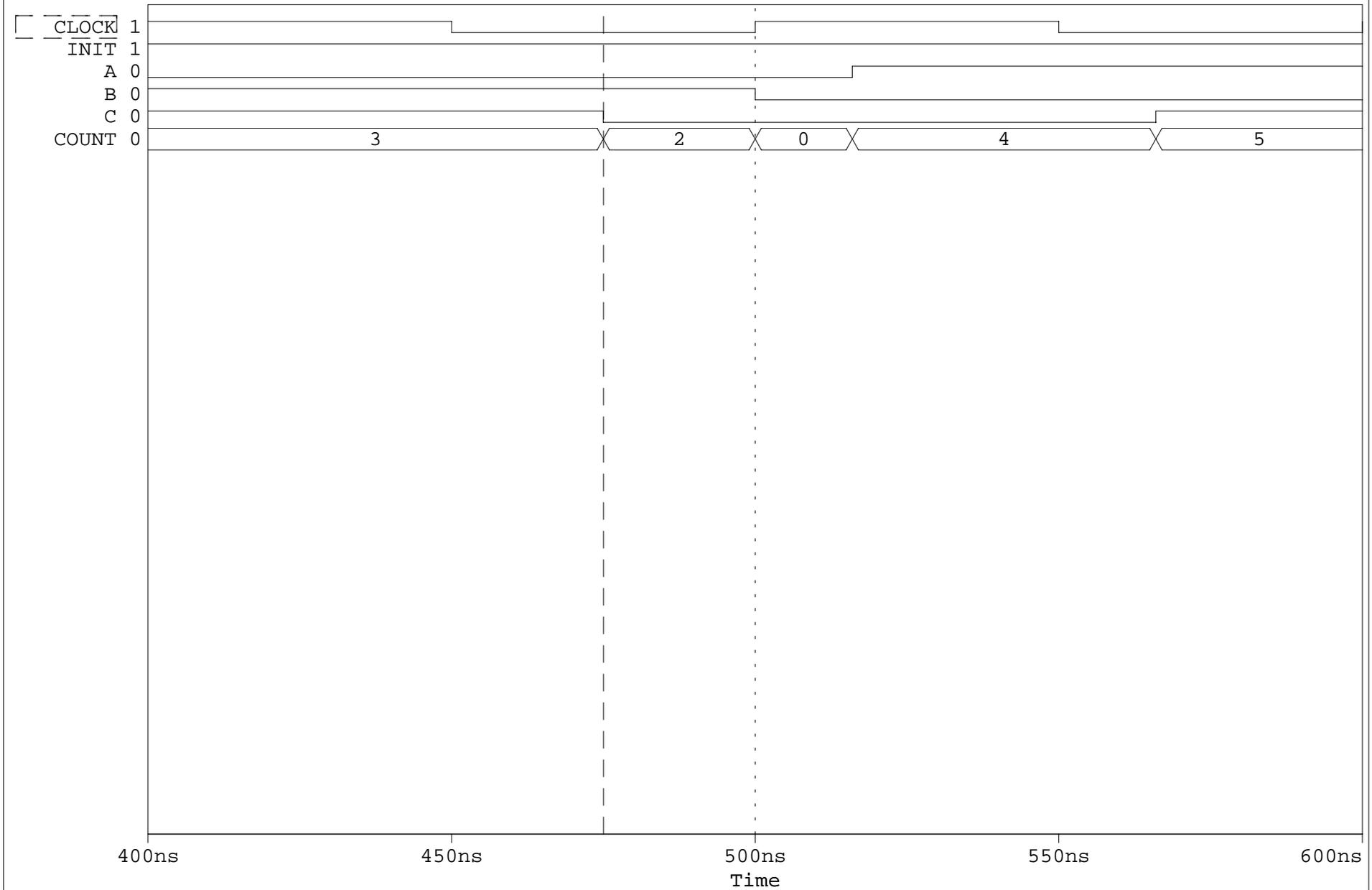


(A) When C goes LO there is a delay before B goes HI. This is T_{pLH} (cursors show it to be about 16ns).



A1:(290.972n),0 A2:(275.000n),0 DIFF(A):(15.972n)

(A) When C goes L0 there is a delay before B goes L0. This is T_{pHL} (cursors show it to be about 25ns).



A1:(500.000n),1 A2:(475.000n),0 DIFF(A):(25.000n)

