EGR 270
Fundamentals of Computer Engineering
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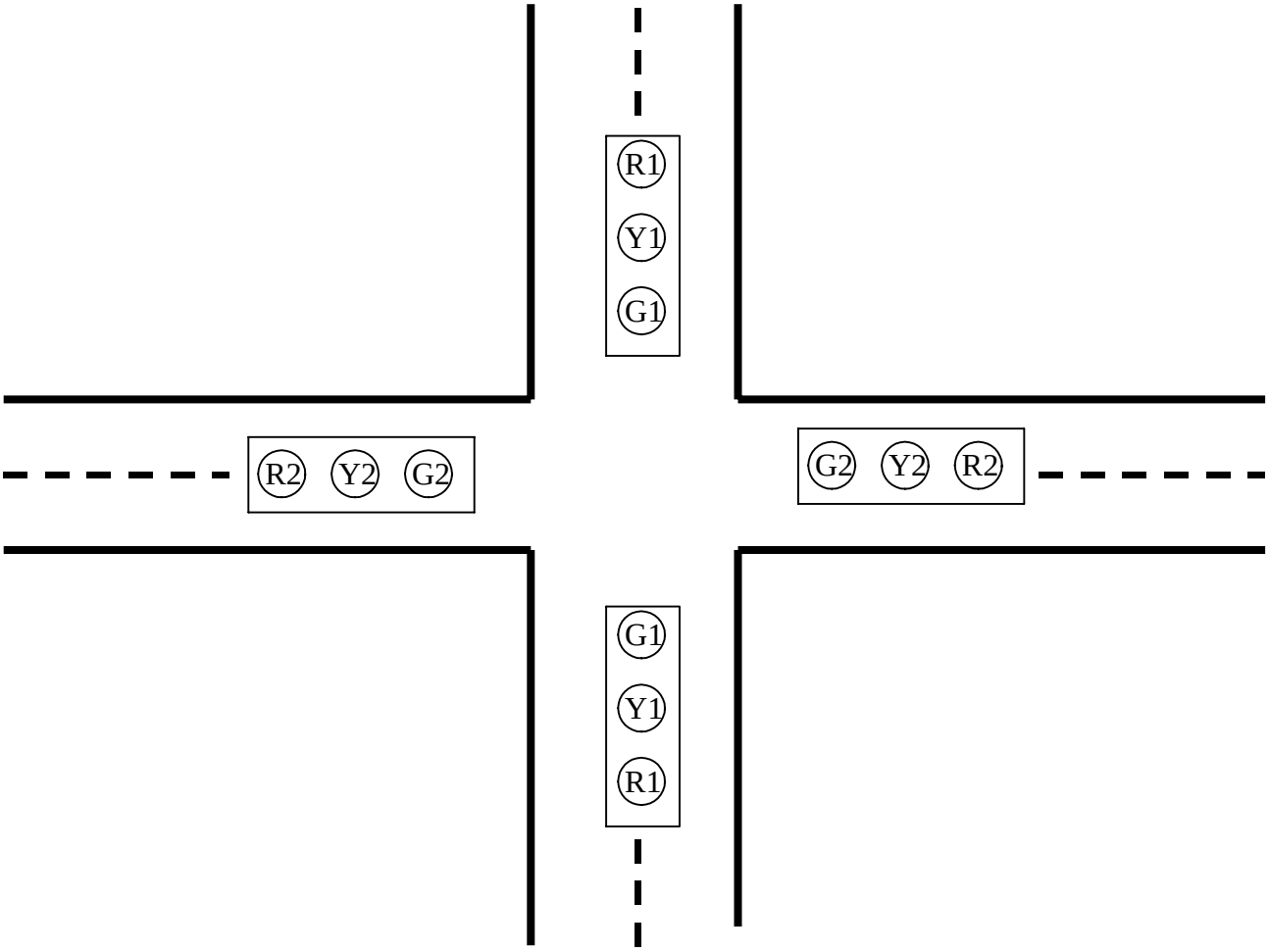
Traffic Light Controller

Problem: Design a circuit to control a traffic light. Assume that the traffic light is at an intersection arranged as shown below. For the North/South (N/S) lanes, the signal names are as follows: R1 = Red, Y1 = Yellow, G1 = Green. Similarly, for the East/West (E/W) lanes, the signal names are R2, Y2, and G2.



Assume that one light cycle takes 16 clock pulses with a clock period, T, of 7 seconds so the time for a complete cycle of all three lights is 16(7) = 112 seconds. The number of clock pulses and the length of time of each light might then be divided up as follows:

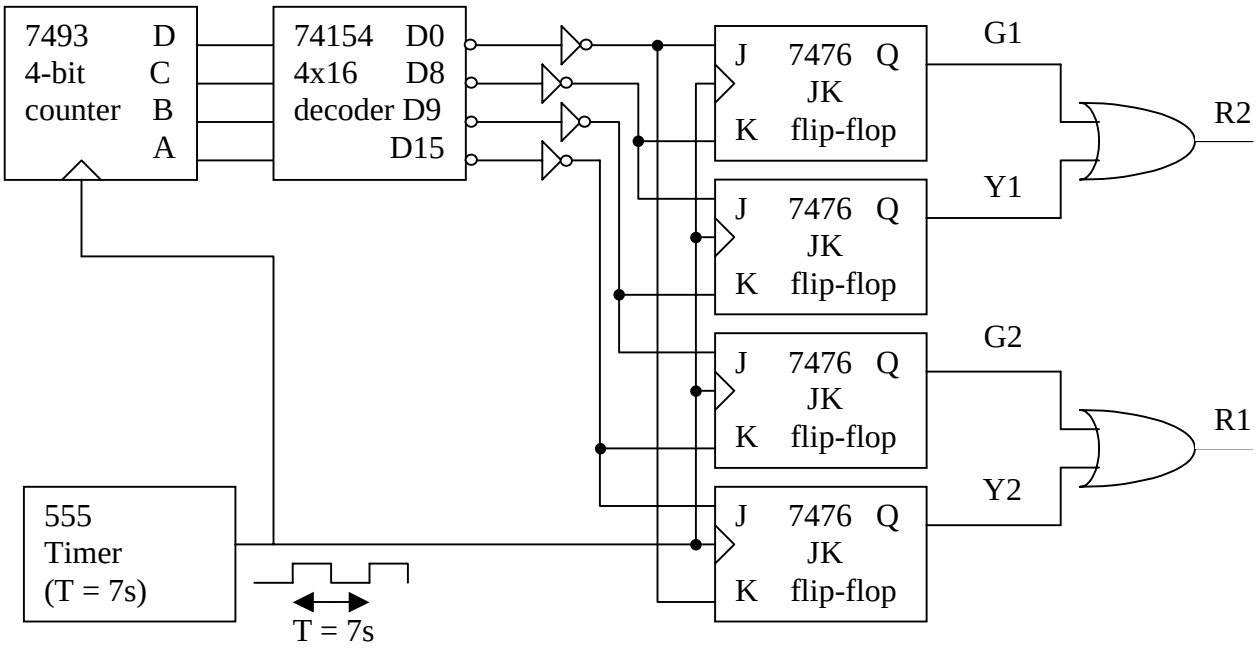
Direction	Light	Number of pulses	Time lit
N/S	R1	7	49 s
N/S	Y1	1	7 s
N/S	G1	8	56 s
E/W	R2	9	63 s
E/W	Y2	1	7 s
E/W	G2	6	42 s

Note that whenever G1 or Y1 is lit, R2 must also be lit.
Similarly, whenever G2 or Y2 is lit, R1 must also be lit.
If G1 and R2 turn on at count 0, then the remaining events can be illustrated by the count number as shown below.

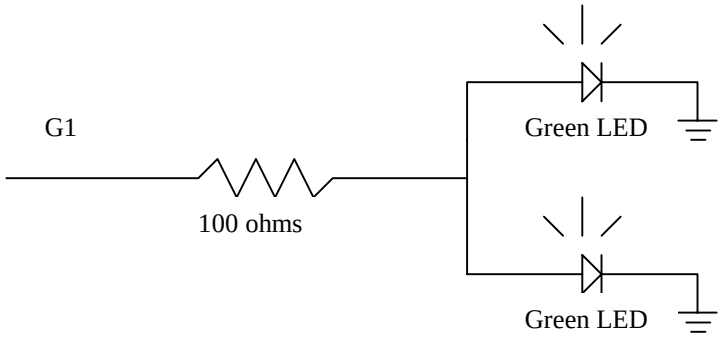
N/S	G1 on							Y1 on	R1 on						
E/W	R2 on								G2 on						Y2 on
Count	0							8	9						15	0

The traffic light controller could now be implemented as follows:

- Use a 555 timer to generate a clock waveform with a period T = 7 seconds.
- Use a 7493 4-bit counter to generate the 16 counts needed
- Use a 74154 4x16 decoder to detect when counts 0, 8, 9, and 15 occur
- Use a 7404 inverter to invert the decoder outputs since the outputs of the 74154 are active-LOW. This will essentially change them to active-HIGH outputs.
- Use 7476 JK flip-flops to toggle the output signals when the correct count occurs.
- Whenever one lane is GREEN or YELLOW, the other lane must be RED, so the four flip-flops can be used to produce the GREEN and YELLOW signals and 7432 OR gates can be used to generate the RED signals.
- See the circuit below and the PSPICE simulation on the following pages



Each output (G1, Y1, R1, G2, Y2, R2) is tied to two LEDs of the appropriate color. For example, G1 drives two lights: one for the North lane and one for the South lane. A 100 ohm current-limiting resistor is used with each output as shown below.



PSPICE Example: Traffic Light Controller

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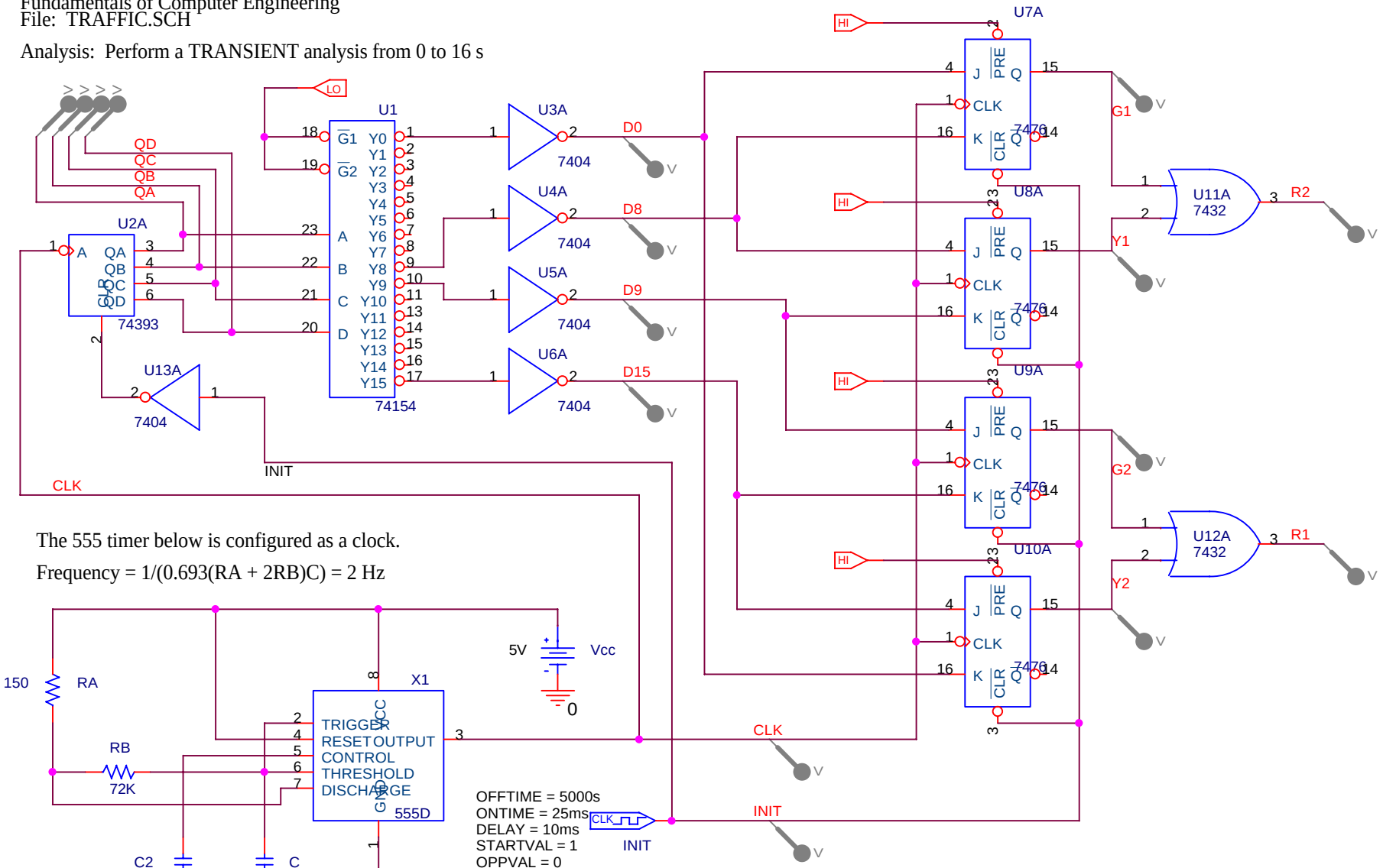
Analysis: Perform a TRANSIENT analysis from 0 to 16 s



The 555 timer below is configured as a clock.

Frequency = 1/(0.693(RA + 2RB)C) = 2 Hz

OFFTIME = 5000s
ONTIME = 25ms
DELAY = 10ms
STARTVAL = 1
OPPVAL = 0

INIT is an active-LOW initialization line for the flip-flops. Note that INIT is inverted to provide an active-HIGH initialization line for the 74383 4-bit counter.

Notes:

1) The BUS {QD,QC,QB,QA};COUNT;D was added as a trace to the output graph so show the output count of the counter in decimal format.

2) Wires were labeled using N1 from the toolbar so that convenient names could be referred to on the graph.

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Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, February 21	Sheet 1 of 1	

** circuit file for profile: Transient

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(A) Timing Diagram for Traffic Light Controller