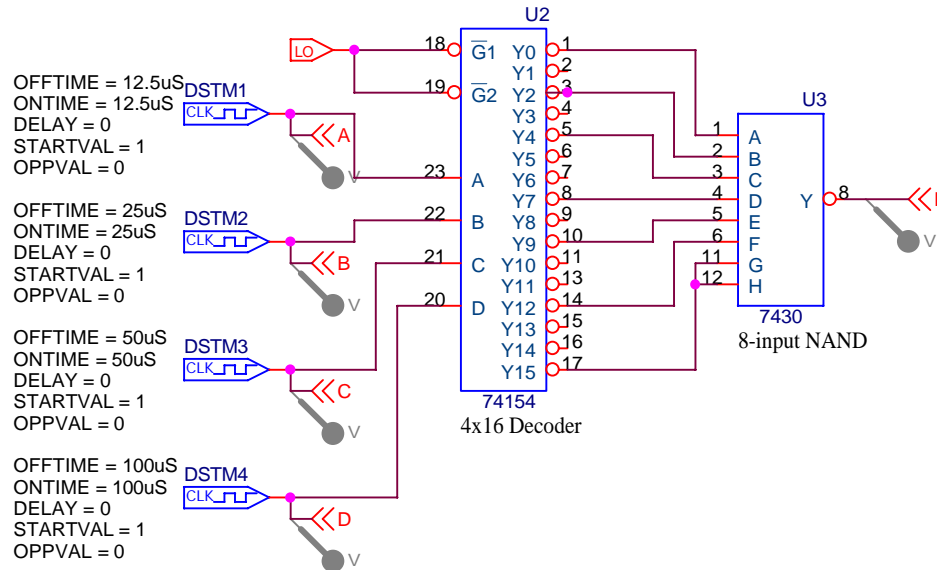


Implementing a Sum of Products expression using a 4 x 16 Decoder

Purpose: Use a 4 x 16 decoder to implement the function $f(D,C,B,A) = \text{Sum}(0,2,4,7,9,12,15)$

Note that the 16 output lines are active-LOW. Since a NAND gate is equivalent to a negative-input OR, the output of the NAND produces a Sum of the (essentially active-HIGH) decoder outputs.

Analysis: Graphing all 16 possible inputs will require a TRANSIENT analysis with a final time of $16(12.5\mu\text{s}) = 200 \mu\text{s}$



Notes:

- 1) The 74154 and 7430 devices are found in the EVAL library.
- 2) The inputs to the circuit are generated using part DigClock from the SOURCE library. The frequency of each clock (or the length of the ONTIME and OFFTIME) are unimportant. The important point is that the period of B is twice the period of A, the period of C is twice the period of B, etc., in order to generate the 16 input combinations in counting order.
- 3) The LO input to the active-LOW enables on the 74154 are generated using the part \$D_LO from the SOURCE library. The easiest way to insert this part is to click on the GND toolbar.
- 4) OFFPAGE symbols (using the <<C toolbar) were used to label the inputs, A, B, C, and D, and the output, F.
- 5) The binary count of the input was displayed on the graph using a BUS. This was done after simulation by selecting ADD - TRACE and then typing in {D,C,B,A};COUNT;D. This means that the signals D,C,B,A are used to form the binary count, the bus was named COUNT, and the count was displayed in Decimal format (D). Use B for binary format, O for octal, and H or X for hexadecimal.

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