EGR 270

Fundamentals of Computer Engineering

File: N270L2

**Lab # 2**

**Logic Gate Characteristics**

**Lab Format**

This is a **Team Lab** so it may be done with a single partner or alone.

If partners are used:

* A single set of Preliminary Work needs to completed **before** lab begins. Preliminary Work will be checked in lab and will be part of the lab report grade.
* A single lab report needs to be submitted.
* Both partners must be present for the entire lab in order to receive credit.

Lab reports will not be accepted until all required circuits have been demonstrated to the instructor.

A. **Objectives**

 The objectives of this laboratory are:

* To become familiar with data sheets for logic gates
* To investigate various logic gate characteristics, including voltage and current levels, loading (fanout), and propagation delay.
* To gain experience in using a logic probe

B. **Materials**

 Breadboard

 Keithley 2230 Triple DC Power Supply (or similar)

 Agilent 33500B Waveform Generator (or similar)

 Tektronix TDS 2002 Digital Storage Oscilloscope (or similar)

 Agilent 33401A Digital Multimeter (Two) – (or similar)

 Digital Logic Probe

 74LS04 Hex Inverter (NOT)

 DIP Switch

 2.2k resistor

C. **Introduction**

 The physical characteristics of logic gates often play an important role in the design of digital circuits. This lab focuses on several of these characteristics, including:

* voltage and current levels
* noise margin
* fanout and loading
* propagation delay

 Each of these physical characteristics are discussed below.

**Current Direction**: According to IEEE standards, ***currents are directed into devices***. Therefore, if a current in a specification is positive, it is entering the device. If a current in a specification if negative, it is leaving the device.

**Voltage and Current Levels**

Several voltage and current levels are of interest when working with logic gates, including:

 VOL = output voltage when the gate is LOW VOH = output voltage when the gate is HIGH

 VIL = input voltage when the gate is LOW VIH = input voltage when the gate is HIGH

 IOL = output current when the gate is LOW IOH = output current when the gate is HIGH

 IIL = input current when the gate is LOW IIH = input current when the gate is HIGH

|  |  |
| --- | --- |
| **Specification** | **7404 NOT** |
| VCC(min) |  |
| VCC(max) | The voltages and currents defined above have fixed values for TTL devices. Check the specification sheet for the 7404 NOT gate during lecture and record the values ..indicated in the table shown below. |
| VIL(max) |  |
| VIH(min) |  |
| VOL(max) |  |
| VOH(min) |  |
| IIL(max)  |  |
| IIH(max)  |  |
| IOL(max)  |  |
| IOH(max)  |  |
| tPLH(max) |  |
| tPHL(max) |  |

**Noise Margins**

VOL(max) is lower than VIL(max) to allow for noise and signal deterioration. Similarly VOH(min) is higher than VIH(min). These differences in voltages are referred to as ***noise margins***. Defined more exactly:

 VNL = LOW level noise margin = VIL(max) - VOL(max)

 VNH = HIGH level noise margin = VOH(min) - VIH(min)

For standard TTL devices:

 VNL = 0.8 V - 0.4 V = 0.4 V

 VNH = 2.4 V - 2.0 V = 0.4 V

These TTL noise margins are illustrated in Figure 1 below:



Figure 1: Noise Margins

**Fanout**

Fanout is the number of standard loads that the output can drive. The number of standard loads is limited by the amount of input current each load requires as compared to the current that the driving gate can deliver. Fanout, therefore, is generally considered to be the smaller of the following two items:

 

Fanout is 10 for standard TTL devices. This is illustrated in Figure 2 below using 7405 NOT gates where the output of the driving gate is LOW. Note that IOL (max) is -16 mA and IIL(max) = -1.6 mA.

1.6 mA (max)

1.6 mA (max)

1.6 mA (max)

1.6 mA (max)

16 mA (max)

**LOW**

10 loads at 1.6mA/load

= 16 mA

Figure 2: Fanout illustrated for a LOW standard TTL output driving 10 loads

Note that IIL(max) = -1.6 mA, but a typical value would be significantly less, so a fanout of 10 is a conservative estimate. A given circuit might be able to drive more 10 loads without exceeding max values for IOL or IOH .

**Propagation Delay**

Propagation delay is the time that it takes a gate to switch logic levels. Logic gates often have a different propagation delay switching from LOW to HIGH than from HIGH to LOW, so two types of delay are defined:

 tPLH = propagation delay when the **OUTPUT** switches from LOW to HIGH

 tPHL = propagation delay when the **OUTPUT** switches from HIGH to LOW

An illustration of each type of propagation delay is shown in Figure 3 below.

Output

Input



Figure 3: Propagation delay illustration

 D. **Preliminary Work**

 Include instructions with each step.

1. Refer to the data sheet for the 7404, 74LS04, and 74S04 and complete the table shown below. Copy this table into the Preliminary Work section of your report. Include sample calculations for determining fanout, VNL, and VNH.

|  |  |  |  |
| --- | --- | --- | --- |
| **Specification** | **7404** | **74LS04** | **74S04** |
| VCC(min) |  |  |  |
| VCC(max) |  |  |  |
| VIL(max) |  |  |  |
| VIH(min) |  |  |  |
| VOL(max) |  |  |  |
| VOH(min) |  |  |  |
| IIL(max)  |  |  |  |
| IIH(max) |  |  |  |
| IOL(max) |  |  |  |
| IOH(max)  |  |  |  |
| tPLH(max) |  |  |  |
| tPHL(max) |  |  |  |
| fanout (min) |  |  |  |
| VNL |  |  |  |
| VNH |  |  |  |

2. Show sample calculations for fanout in the table above.

3. Show sample calculations for VNL and VNH in the table above.

4. Include a pinout for the 74LS04

E. **Laboratory Work**

 1. **Measurement of Voltages and Currents**

* Fill out the specified values in table shown below using the 74LS04 data sheet (or from the Preliminary Work section). Include the word MIN or MAX with each specification.
* Construct Circuit 1 using a 74LS04 IC.
* Apply a HIGH input (using a DIP switch as shown) to the first gate (thus the output is LOW) and measure the input current (IIL) to the second gate and the output voltage (VOL) of the first gate using a digital multimeter.
* Repeat the measurements with a LOW input to the first gate (thus the output is HIGH) and measure the input current (IIH) to the second gate and the output voltage (VOH) of the first gate.
* Record the results (with 3 significant digits if available from the meter) in the table below and verify that these values are within specified limits.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Measured Value | Specified Value | Within Specs? |
| IIL­ |  |  |  |
| VOL |  |  |  |
| IIH |  |  |  |
| VOH |  |  |  |

* Ask the instructor to look at the results above to be sure that they look correct.

2.2k

5V

(No connection)

Ammeter

Voltmeter

**Circuit 1**

2. **Logic Probes**

Connecting the logic probe to HIGH or LOW points on a circuit will result in different colored LEDs lighting and different sounds from the probe.

* Practice using a logic probe on Circuit 1 by checking a HIGH voltage (on pin 14) and a LOW voltage (on pin 7). Record the lights lit and sounds made in the table below.

|  |  |  |
| --- | --- | --- |
| Use Logic Probe to measure | Color LED lit | Sound made (high pitch or low pitch) |
| HIGH Voltage (pin 14) |  |  |
| LOW voltage (pin 7) |  |  |

* Next use a logic probe to check the inputs and outputs on an unused gate on the 74LS04 (no wires connected to the input or output, but powered up). Complete the table below.

|  |  |
| --- | --- |
| Use Logic Probe to measure | Results (LOW, HIGH, or NO READING) |
| Open input |  |
| Open output |  |

* Record the truth table for a 74LS04 NOT gate below. Include the truth table in your report.

|  |  |
| --- | --- |
| A | A’ |
| 0 |  |
| 1 |  |

* Based on the truth table above and your results using a logic probe on an unused gate, complete the following statement (and include the statement in your lab report):

***Since the open output of the 74LS04 read \_\_\_\_\_\_\_\_\_\_, it can be stated that “OPEN INPUTS FOR 74LS SERIES GATES ACT LIKE \_\_\_\_\_\_\_\_\_\_ .”***

* Based on your results, which of the following two statements is correct? Include the correct statement in your lab report.
	+ ***Open inputs on TTL gates float LOW.***
	+ ***Open inputs on TTL gates float HIGH.***

3. **Propagation Delay Measurement** (Note: The instructor may set up this step as a demonstration. If so, be sure to get a printout of the waveforms showing tPHL and tPLH. Clearly label tPHL and tPLH exactly where they are measured on the printouts and label the input and the output.

* Measure tPLH: Construct Circuit 2 shown below using the function generator and oscilloscope settings indicated below. Turn on the oscilloscope before turning on the computer and then run program **WaveStar for Oscilloscopes**. View both waveforms A and B on the oscilloscope and adjust the time scale until you can see tPLH . Add two time cursors at the 50% points on waveforms and the difference between the cursors (also displayed) will be tPLH. Capture the image with WaveStar and print it or cut and paste the images to Word. Clearly label (by hand) where tPLH is measured on the printed waveform. Also label the input and the output on the printout. Include the printout in your report.
* Repeat the step above to measure tPHL .
* Compare the measured values to values found in the spec. sheet (see table below).
* Ask the instructor to look at the your results to be sure that they look correct.

 Use the following settings for the function generator and the oscilloscope. (Note: Pressing ***AUTO SET*** on the oscilloscope will typically result in the correct settings!)

|  |  |  |
| --- | --- | --- |
| **Tektronix TDS 2002 Oscilloscope** |  | **Agilent 33500B Waveform Generator** |
| **Control** | **Setting** |  | **Control** | **Setting** |
| Ch. 1/Ch. 2 Menu | *Coupling: DC* |  | Waveform |  (square wave) |
|  | *BW limit: OFF* |  | Frequency \* | 100 kHz |
|  | *V/div: Coarse* |  | Amplitude \* | 5 Vpp |
|  | *Probe: 1X* |  | Offset \* | 2.5 V |
|  | *Invert: Off* |  |  |
| Trigger Menu | Type: Edge |  | \* Enter the value and then a choice of units will |
|  | Source: Ch. 1 |  | be shown using the buttons under the screen). |
|  | Slope: Rising |  |  |  |
|  | Mode: Auto |  |  |  |
|  | Coupling: DC |  |  |  |
| Ch.1 V/div | 1V |  |  |  |
| Ch. 2 V/div | 1V |  |  |  |



Circuit 2: Measurement of tPHL and tPLH

|  |  |  |  |
| --- | --- | --- | --- |
|  | Measured Value | Specified Value | Within Specs? |
| tpHL |  |  |  |
| tpLH |  |  |  |

**Report**

Do not use part of this lab guide as part of your report. Create your report from scratch.

Remember that each lab report should have the following four sections. See additional notes below.

**Title Page**

**Preliminary Work**

* Include instructions

**Lab Results**

* Include all measured results. Use tables to summarize results whenever possible. (Do not simply fill in the sheet from the lab guide. This is not acceptable.)
* Include step numbers and titles or headings that make it clear what is being shown.
* Include units whenever appropriate.

**Discussion/Conclusion**

* Discuss each part of the experiment performed in lab.
* Are the results as expected? Were all results withing specifications? If any results were not within specifications, discuss possible reasons.
* What have you proven or demonstrated by completing each step of the experiment?
* Explain any errors.