**Semester: Spring 2020**

**Section: D01B (Lecture MW 4:20 – 5:35pm in H-164, Lab W 1:00-3:00pm in H-273)**

EGR 270

Fundamentals of Computer Engineering

Instructor: Paul Gordy

# Course Schedule (Tentative)

The following course schedule may change during the progression of the course. The course schedule may change at the discretion of the instructor; however, students will be notified in writing (email) when any changes/additions are made to the schedule.

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| Date | Lecture Topic | Reading | Assignments Due | Lab |
| Jan | M, 13 | Digital systems. Number systems (decimal, binary, octal, hexadecimal). Expansion by place value. Converting between bases. Arithmetic operations in various bases. | Ch. 1Lecture #1 |  | - - - - - |
|  | W, 15 | Complements (r’s and r-1’s). Binary codes. Decimal codes. Parity and error detection. Alphanumeric Codes. ASCII code. UniCode. UTF-8. | Ch. 1Lecture #1 |  | No lab meeting |
|  | M, 20 | TCC closed. Martin Luther King, Jr. Day |  |  | - - - - - |
|  | W, 22 | Boolean algebra. Postulates, theorems and operators. Minimizing Booleans expressions. | Ch. 2Lecture #2A |  | Lecture for Lab 1. PSPICE and Fritzing demo. |
|  | M, 27 | Minterms, maxterms, Sum of Products (SOP), Product of Sums (POS). Literals. Standard and non-standard forms. Basic logic gates. | Ch. 2Lecture #2A | HW #1 |  |
|  | W, 29 | Karnaugh Maps (Kmaps). 2-5 variables.  | Ch. 2Lecture #2B |  | Perform Lab 1. Lecture for Lab 2. |
| Feb | M, 3 | Prime implicants, essential prime implicants. Don’t cares. Forming SOP and POS expressions from Kmaps.  | Ch. 2Lecture #2B |  | - - - - - |
|  | W, 5 | XOR expressions from Kmaps. Cost criteria. Propagation delay. Minimizing multiple-output circuits. | Ch. 2Lecture #2B | HW #2 | Perform Lab 2. Report for Lab 1 due. |
|  | M, 10 | Combinational logic circuits. Design hierarchy. Design procedure. | Ch. 3Lecture #3A |  | - - - - - |
|  | W, 12 | 7-segment displays and decoders. Common cathode vs common anode. Unused inputs. Commercial devices. | Ch. 3Lecture #3A | HW #3 | Lecture for Lab 3. PSPICE Demo: Analysis of combinational logic circuits |
|  | M, 17 | Decoders, encoders. Enables. Active-HIGH vs active-LOW. Functional blocks. Implementing Boolean functions using decoders. Applications.  | Ch. 3Lecture #3B |  | - - - - - |
|  | W, 19 | Priority encoders, magnitude comparators. | Ch. 3Lecture #3B |  | **Test #1 (Ch 1-2, HW #1-3)** |
|  | M, 24 | Multiplexers, demultiplexers. Implementing Boolean functions using multiplexers.  | Ch. 3Lecture #3B | HW #4 | - - - - - |
|  | W, 26 | Programmable logic devices (PLDs). PAL, PLA. | Ch. 5.2Lecture #3C |  | Perform Lab 3 – Week 1/2Report for Lab 2 due. |
| Mar | M, 2 | Arithmetic operations. Half & full adders. N-bit adders. Fast carries. | Ch. 3Lecture #3C |  | - - - - - |
|  | W, 4 | Signed numbers. Subtraction using r’s complement addition. Adder/subtractor circuit. Incrementers and decrementers. Contraction. | Ch. 3Lecture #3C | HW #5 | Perform Lab 3 – Week 2/2 |
|  |  | Spring break. No class week of March 9-14. |  |  |  |
|  | M, 16 | Intro to VHDL and FPGAs. | Intro to VHDL |  | - - - - - |
|  | W, 18 | Intro to VHDL and FPGAs. Implementing combinational circuits. Discuss Lab 5. | Intro to VHDL | HW #6 | Perform Lab 4. Report for Lab 3 due. |
|  | M, 23 | Synchronous sequential Logic Circuits. SR latch. Flip-flops (SR, JK, D, and T). Triggering. Asynchronous inputs. | Ch. 4Lecture #4A | PSPICE #1 | - - - - - |
|  | W, 25 | State diagrams and state tables. State assignment. Mealy and Moore machines. Design by the excitation table method. | Ch. 4Lecture #4A |  | **Test #2 (Ch 3, 5.8, HW #4-6)** |
|  | M, 30 | PSPICE analysis of a sequential circuit. Unused states. | Ch. 4Lecture #4A |  | - - - - - |
| Apr | W, 1 | Counters: counting events, frequency division and timing sequences. Self-starting counters. | Ch. 4Lecture #4A | HW #7 | Perform Lab 5. Report for Lab 4 due. |
|  | M, 6 | Mealy vs Moore machines – review. Sequence detectors. State equations. Flip-flop characteristic equations. | Ch. 4Lecture #4B |  | - - - - - |
|  | W, 8 | Design by state equations.  | Ch. 4Lecture #4B |  | Perform Lab 6 – Week 1/2Report for Lab 5 due. |
|  | M, 13 | Design using the one-hot method. | Ch. 4Lecture #4B |  | - - - - - |
|  | W, 15 | More on VHDL and FPGAs. Implementing sequential circuits. Discuss Lab 7. | More on VHDL | HW #8 | Perform Lab 6 – Week 2/2 |
|  | M, 20 | Computer architecture. Microcontrollers, instruction set architecture, RISC machines, memory types, Harvard vs von Neumann architecture. Memory maps. ATMega328P architecture. | Computer Architecture, Microcontrollers and Assembly Language | PSPICE #2 | - - - - - |
|  | W, 22 | Assembly language. ATMega328P and AVR assembly language. Addressing modes. Registers. Status register and branching. Atmel Studio 7 software. | Computer Architecture, Microcontrollers and Assembly Language |  | Perform Lab 7.Report for Lab 6 due |
|  | M, 27 | Atmel Studio 7 software. Assembling and simulating. Viewing registers and registers. Inputs/outputs on the ATmega328P. Pin mapping to the Arduino Nano. Discuss Lab 8. Pass out **Test #3** (take-home test on Chapter 4 and AVR assembly language) | Atmel Studio 7 Tutorial |  | - - - - - |
|  | W, 29 | Asynchronous circuits/ripple counters. |  |  | Perform Lab 8 (no report)Report for Lab 7 due. |
| May | M, 4 | Shift registers. Serial transfer, parallel transfer, rotation of data. Tri-state devices. Test #3 due. | Asynchronous circuits/shift registers | HW #9 | - - - - - |
|  | W, 6 | Final Exam – comprehensive | Asynchronous circuits/shift registers |  | Last day to submit any late PSPICE assignments or lab reports. |