EGR 277 Due date: _____
Fundamentals of Computer Engineering (See Due Dates Table)
File: N270P2A

PSPICE Assignment #2

PSPICE Analysis of Sequential Logic Circuits

Reference:

Sample PSPICE Report
PSPICE Example: "***Modified Sequence Counter***" (File: MOD_SEQ.OPJ)

Assignment Description:

Use Cadence Capture version 16 or later for this assignment.

1. Custom Modified Sequence Counter:

A. Design a modified sequence counter using JK flip-flops that will count out the following sequence: The first four unique digits in your StudentID (not including the digit 9) followed by the digit 9 and then repeat. If you do not have 4 unique digits, then add in as many of the follow digits as you need: 7, 2, 6, 8. Several examples are shown below.

StudentID	Counting Sequence
2869834	2, 8, 6, 3, 9, and repeat
2662518	2, 6, 5, 1, 9, and repeat
2552525	2, 5, 7, 6, 9, and repeat

Treat all unused counts as "don't cares." Use the Excitation Table method for your design. Neatly show all steps in your design. ***Note that this is the same sequence used in Lab 6***.

B. Use PSPICE to simulate the circuit above. Use a 10 kHz clock to run the counter and use another clock to initialize the counter to the 1st count in your sequence. Generate a timing diagram using PROBE that shows 10 cycles of the 10 kHz clock as well as the initialization signal and the outputs. Also add a bus within PROBE which gives the decimal value of the count.

C. Zoom in on a small portion of the first cycle in the timing diagram above and print a new timing diagram that clearly illustrates the effect of the initialization signal.

D. Change the frequency of the 10 kHz clock in part B to 25 MHz and again generate a timing diagram that shows 10 cycles of the clock as well as the initialization line, output signals, and the bus specifying the count. Is the count correct at all times? Discuss the results in your report.

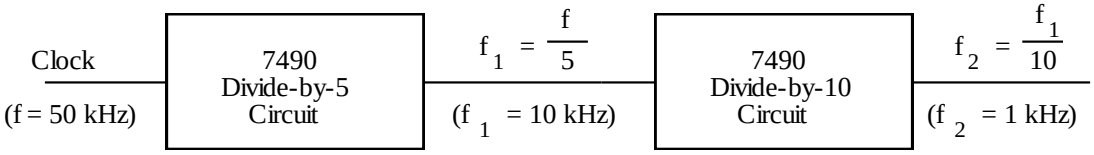
E. Repeat step 1B with the 10 kHz clock replaced by a clock generator using a 555 timer with a frequency equal to the last 4 non-zero digits of your StudentID in Hz (any duty cycle is OK). Show all steps illustrating how you selected R_A, R_B, and C. Using your values of R_A, R_B, and C, show the calculations for T_L, T_H, T, D, and f in your report (or on the schematic). Adjust the time for the transient response so that 10 cycles of the count are again displayed. Use two cursors to measure the period T of the clock and add labels to the graph displaying the measured values of T and f. Include a table comparing your designed frequency and the frequency measured in PSPICE and % error.

F. Include a Discussion section. Discuss steps 1B through 1E.

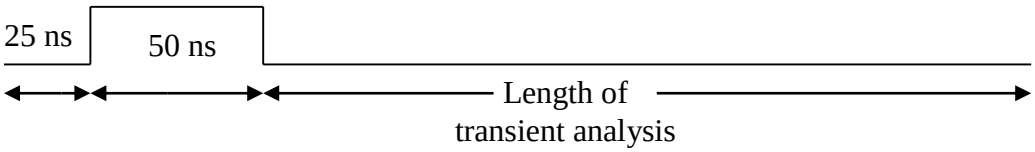
(continued)

2. Frequency Division Using 7490 Decade Counters:

A. Use PSPICE to connect two 7490 decade counters as shown below. The first counter should be configured as a divide-by-five circuit and the second counter as a divide-by-ten circuit with a symmetric output (50% duty cycle). Use a clock input with a frequency of 50 kHz. Hint: To properly initialize the counter, apply a LO input to R91 and R92 and apply an initialization pulse to R01 and R02. The initialization signal should go HIGH for at least twice the length of the propagation delay of the 7490 (or 2 x 25 ns = 50 ns) as shown below.



Initialization signal:



B. Generate a timing diagram within PROBE showing the waveforms f, f_1, and f_2. Show 50 cycles of f (this should correspond to 10 cycles of f_1, and 1 cycle of f_2).

C. Discuss the results.

Extra Credit:

D flip-flop design and simulation: (worth up to 25 extra points on this assignment)
Repeat Problem 1 (parts A and B only) using D flip-flops (7474) designed using the state equation method. Show all of your design work.
Include a Discussion Section. Discuss the results and compare the results to the circuit designed using JK flip-flops. Which circuit was easier to design? How many flip-flops and logic gates were required for each design?