EGR 270 Due date: _____
Fundamentals of Computer Engineering (See Due Dates Table)
File: N270P1A

PSPICE Assignment #1

PSPICE Analysis of Combinational Logic Circuits

Reference:

Handout: Sample PSPICE Report
PSPICE Example: "***Combinational Logic Circuit***" (File: LOGIC1.OPJ)
PSPICE Example: "***Implementing Functions with a 4 x 16 Decoder***" (File: DECODER.OPJ)

Assignment Description:

Use Cadence Capture version 16.5 or later for this assignment.

1. **Custom Combinational Logic Circuit:**

A certain function f is defined as follows:

f(A, B, C, D) = Σ(first 5 unique digits of your StudentID + minterms 12 and 15).

Example: If your StudentID is 2286435 then your first 5 unique digits are 2, 8, 6, 4, and 3, so f is defined as follows: f(A, B, C, D) = Σ(2, 3, 4, 6, 8, 12, 15). If your StudentID has less than 5 unique digits, add minterm(s) 10 and/or 14.

Let binary waveforms for A, B, C, and D be defined as follows:

A - Clock with a frequency of 5 kHz, initial value is LOW
B - Clock with a frequency of 10 kHz, initial value is LOW
C - Clock with a frequency of 20 kHz, initial value is LOW
D - Clock with a frequency of 40 kHz, initial value is LOW

The 4 waveforms A,B,C,D represent a 4-bit binary code that varies from 0 to 15 in order.

A. SOP Implementation:

1) Determine by hand a minimal Sum Of Products (SOP) expression for the function f described above using a Karnaugh map.
2) Use PSPICE to implement the SOP expression above using only AND, OR and NOT gates. Use Digital Clocks for A, B, C, and D as described above. Add labels to define all inputs and outputs by standard names. Add text to ***all PSPICE schematics***, including name, course, assignment number, problem number, and a brief description.
3) Analyze the circuit and create a graph of A, B, C, D, and f above as well as a bus defining the decimal value of the 4 waveforms {A, B, C, D}. The length of the timing diagram should be such that all 16 possible combinations of A, B, C, and D are shown in order. Verify that f is HIGH for each minterm as described above. Include an appropriate title on the graph, such as **"SOP implementation of f(A,B,C,D) = Sum(your minterms)**".
4) Discuss the results.

B. POS Implementation:

Repeat part 1A above for a Product Of Sums (POS) implementation of f.

C. 8x1 Multiplexer Implementation:

1) Use a ***multiplexer implementation table*** by hand to determine the appropriate connections to be used in order to implement the function f described above. Be aware that A is the MSB and D is the LSB. Add labels to define all inputs and outputs by standard names.
2) Use PSPICE to implement the multiplexer circuit above using 74151A 8x1 multiplexer. Use Digital Clocks for A, B, C, and D as described above.
3) Analyze the circuit and graph A, B, C, D, and f above as well as a bus defining the decimal value of the 4 waveforms {A, B, C, D}. The length of the timing diagram should be such that all 16 possible combinations of A, B, C, and D are shown in order. Verify that f is HIGH for each minterm as described above. Include an appropriate title on the graph.
4) Discuss the results.

D. 4 x 16 Decoder Implementation:

1) Implement either the SOP function of part A or the POS function of part B using two 3x8 decoders (using two 74155 IC's) to form a 4 x 16 decoder. Add labels such as D0, D2, etc., to all used decoder outputs
2) Analyze the circuit and graph A, B, C, D, f, all used decoder outputs, and a bus defining the decimal value of the 4 waveforms {A, B, C, D}. The length of the timing diagram should be such that all 16 possible combinations of A, B, C, and D are shown in order. Verify that f is HIGH for each minterm as described above. Include an appropriate title on the graph.
3) Discuss the results. Do the used decoder outputs (D0, D1, etc) appear as expected? Explain.

E. Comparison of parts 1A, 1B, 1C, and 1D:

Compare the results of parts 1A, 1B, 1C, and 1D. Were they all identical? Which method do you prefer?

2. **4-Bit Magnitude Comparator:**

Use PSPICE to implement a 4-bit magnitude comparator circuit using a 7485. Add 4 clocks to the schematic defined as follows:

A - Clock with a frequency of 5 kHz, initial value is LOW
B - Clock with a frequency of 10 kHz, initial value is LOW
C - Clock with a frequency of 20 kHz, initial value is LOW
D - Clock with a frequency of 40 kHz, initial value is LOW

Connect the waveforms to the inputs indicated below:

A3 - Clock A (MSB)	B3 - Clock D (MSB)
A2 - Clock B	B2 - Clock B
A1 - Clock C	B1 - Clock A
A0 - Clock D	B0 - Clock C

Note that the magnitude comparator will be comparing the binary value of ABCD with the binary value of DBAC.

Use PROBE to form a timing diagram of A, B, C, D, and the 3 magnitude comparator outputs (in order). Also show two buses, one defining the decimal value of {A, B, C, D} and the other defining the decimal value of {D, B, A, C}. The length of the timing diagram should be such that all 16 possible combinations of A, B, C, and D can be seen in order. Verify that the magnitude comparator yields the correct results in each case. ***Clearly discuss the output graph. Explain how the output graph shows that the circuit is performing properly.***