EGR 270
Fundamentals of Computer Engineering
File: N270O2

Test #2 Overview

Related Homework Assignments: Homework # 4 - 6
Related textbook sections: Chapter 3 and Chapter 5, Section 2 on PLAs and PALs in Logic and Computer Design Fundamentals, 5th Ed., by Mano

Ch. 3 - Combinational Logic Design

Design Procedure:

- Naming the exact steps is not important – just be able to design a circuit
- Design problems – be able to design a custom combinational logic circuit
- Codes will be provided for code converter problems (except you should know the BCD code)

Technology mapping – be able to implement circuits using AND-OR-NOT gates, XOR gates, decoders, multiplexers, PLDs, etc.
BCD-to-7-segment decoders

- common anode versus common cathode
- segment labeling (a-g)
- design of decoder circuit

Other common combinational logic circuits:

- Magnitude Comparators
- Decoders
- Encoders
- Priority Encoders
- Multiplexers
- Demultiplexers

For the devices above:

- Be able to work with active-LOW or active-HIGH inputs, outputs, enable lines, etc.
- Be familiar with the devices as block diagrams or as circuits.
- Be able to design the circuits, extend block diagrams, read or develop truth tables, etc.
- Know what inputs and outputs to expect for a given device.
- Be able to read specification sheets

Implementing Boolean expressions using:

- Decoders (using minterms or maxterms)
- Multiplexers (implementing a function of N+1 variables using a MUX with N select lines)

Timing diagrams – Given the input waveforms for a specified device, sketch the output waveforms

Ch. 3 - Arithmetic Functions and Circuits

Half-adder
Full-adder
N-bit adders
Carry look-ahead circuit (general information)
Representation of negative numbers in 2's complement form
Subtraction using r's complement addition
Signed arithmetic (adding or subtracting signed numbers)
Adder-subtractor circuit
Contraction – modifying an existing circuit or function to create a related (and simpler) circuit or function. Example: Given an N-bit adder using full adders, be able to use contraction to form:

- Incrementer

- Increment-by-N circuit

Ch. 5, Section 2 – Programmable Logic Devices

Programmable Logic Devices (PLD's)

- General information
- PLAs and PALs
- Implement Boolean expressions using logic array diagrams like Fig. 5-8 and 5-10 in the text

Items NOT included on this test:

Implementing a circuit with only NANDs or NORs:
Hardware Description Languages (HDLs) - our main focus will be using HDL in lab
Subtraction using (r-1)'s complement addition