EGR 270
Fundamentals of Computer Engineering
File: N270L2

Lab # 2

Logic Gate Characteristics

Lab Format

This is a **Team Lab** so it may be done with a single partner or alone.
If partners are used:

- A single set of Preliminary Work needs to completed **before** lab begins. Preliminary Work will be checked in lab and will be part of the lab report grade.
- A single lab report needs to be submitted.
- Both partners must be present for the entire lab in order to receive credit.

Lab reports will not be accepted until all required circuits have been demonstrated to the instructor.

A. Objectives

The objectives of this laboratory are:

- To become familiar with data sheets for logic gates
- To investigate various logic gate characteristics, including voltage and current levels, loading (fanout), and propagation delay.
- To become familiar with the difference between logic gates with totem-pole outputs and open-collector outputs.
- To investigate the uses of open-collector gates
- To use open-collector gates to provide higher output voltage levels
- To use open-collector gates and output transistors to provide high current levels for loads

B. Materials

Breadboard
Keithley 2230 Triple Challen DC Power Supply (or similar)
Agilent 33500B Waveform Generator (or similar)
Tektronix TDS 2002 Digital Storage Oscilloscope
Agilent 33401A Digital Multimeter (Two)
Micronta Digital Logic Probe
74LS00 Quad 2-input NAND IC (totem-pole outputs)
7401 Quad 2-input NAND IC (open-collector outputs)
74LS06 or 7416 Hex Inverter Buffer/Driver (open collector)
TIP32C PNP transistor (or similar)
12V Automobile Marker Bulb (#194)
12V DC Motor (12,500 rpm)

C. Introduction

The physical characteristics of logic gates often play an important role in the design of digital circuits. This lab focuses on several of these characteristics, including:

- voltage and current levels
- noise margin
- fanout and loading
- propagation delay

Each of these physical characteristics are discussed below.

Current Direction: According to IEEE standards, ***currents are directed into devices***. Therefore, if a current in a specification is positive, it is entering the device. If a current in a specification if negative, it is leaving the device.

Voltage and Current Levels

Several voltage and current levels are of interest when working with logic gates, including:

- V_{OL} = output voltage when the gate is LOW
- V_{OH} = output voltage when the gate is HIGH
- V_{IL} = input voltage when the gate is LOW
- V_{IH} = input voltage when the gate is HIGH
- I_{OL} = output current when the gate is LOW
- I_{OH} = output current when the gate is HIGH
- I_{IL} = input current when the gate is LOW
- I_{IH} = input current when the gate is HIGH

Specification	7400 NAND
V_{CC}(min)	
V_{CC}(max)	
V_{IL}(max)	
V_{IH}(min)	
V_{OL}(max)	
V_{OH}(min)	
I_{IL}(max)	
I_{IH}(max)	
I_{OL}(max)	
I_{OH}(max)	
t_{PLH}(max)	
t_{PHL}(max)	

The voltages and currents defined above have fixed values for TTL devices. Check the specification sheet for the 7400 NAND during lecture and record the values

Noise Margins

V_{OL}(max) is lower than V_{IL}(max) to allow for noise and signal deterioration. Similarly V_{OH}(min) is higher than V_{IH}(min). These differences in voltages are referred to as ***noise margins***. Defined more exactly:

V_{NL} = LOW level noise margin = V_{IL}(max) - V_{OL}(max)

V_{NH} = HIGH level noise margin = V_{OH}(min) - V_{IH}(min)

For standard TTL devices:

V_{NL} = 0.8 V - 0.4 V = 0.4 V

V_{NH} = 2.4 V - 2.0 V = 0.4 V

These TTL noise margins are illustrated in Figure 1 below:

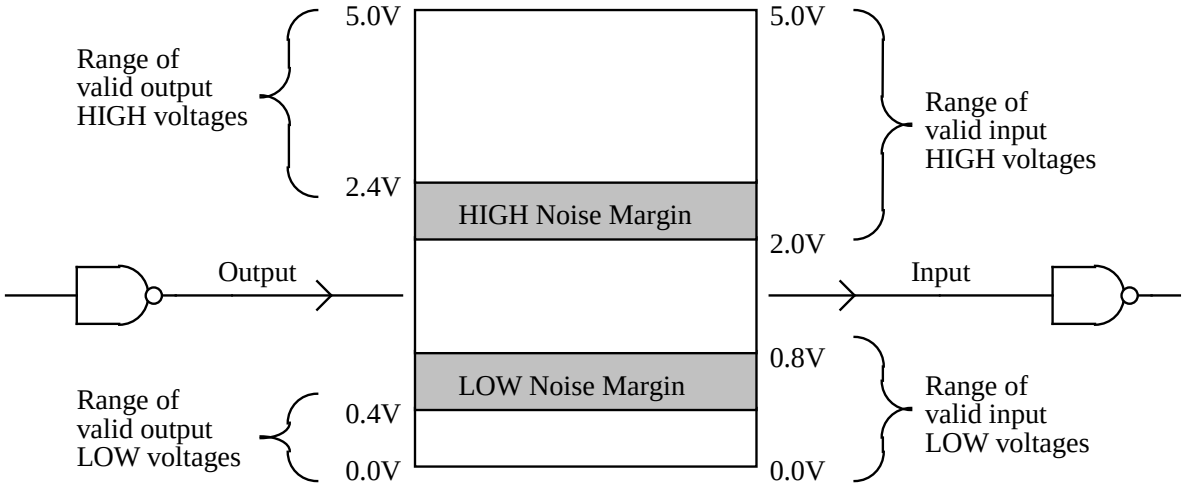


Figure 1: Noise Margins

Fanout

Fanout is the number of standard loads that the output can drive. The number of standard loads is limited by the amount of input current each load requires as compared to the current that the driving gate can deliver. Fanout, therefore, is generally considered to be the smaller of the following two items:

$$\text{fanout} = \frac{I_{OL}(\text{max})}{I_{IL}(\text{max})} \quad \text{or} \quad \text{fanout} = \frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$$

Fanout is 10 for standard TTL devices. This is illustrated in Figure 2 below using 7400 NANDs (with their inputs tied together to act as inverters) where the output of the driving gate is LOW. Note that I_{OL} (max) is -16 mA and I_{IL}(max) = -1.6 mA.

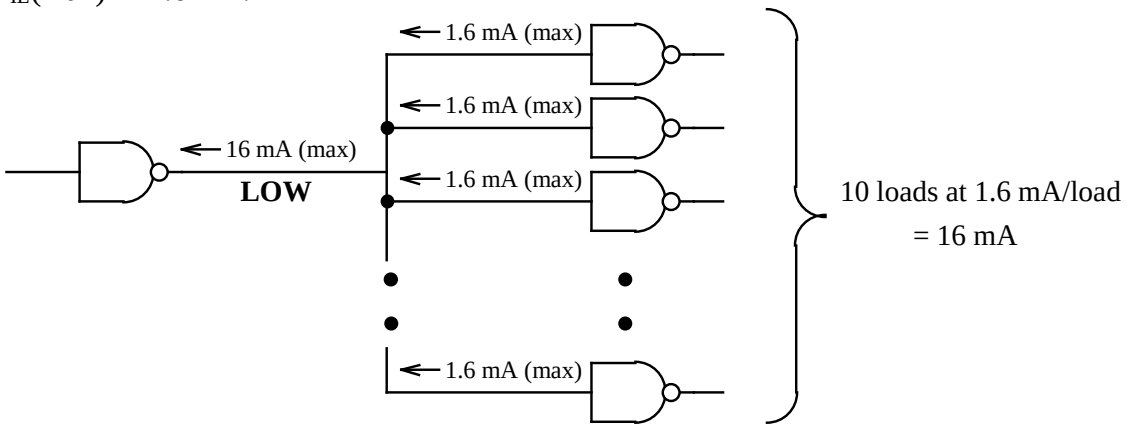


Figure 2: Fanout illustrated for a LOW TTL output driving 10 loads

Note that I_{IL}(max) = -1.6 mA, but a typical value would be significantly less, so a fanout of 10 is a conservative estimate. A given circuit might be able to drive more actual loads than 10 without exceeding max values for I_{OL} or I_{OH} .

Propagation Delay

Propagation delay is the time that it takes a gate to switch logic levels. Logic gates often have a different propagation delay switching from LOW to HIGH than from HIGH to LOW, so two types of delay are defined:

t_{PLH} = propagation delay when the **OUTPUT** switches from LOW to HIGH

t_{PHL} = propagation delay when the **OUTPUT** switches from HIGH to LOW

An illustration of each type of propagation delay is shown in Figure 3 below.

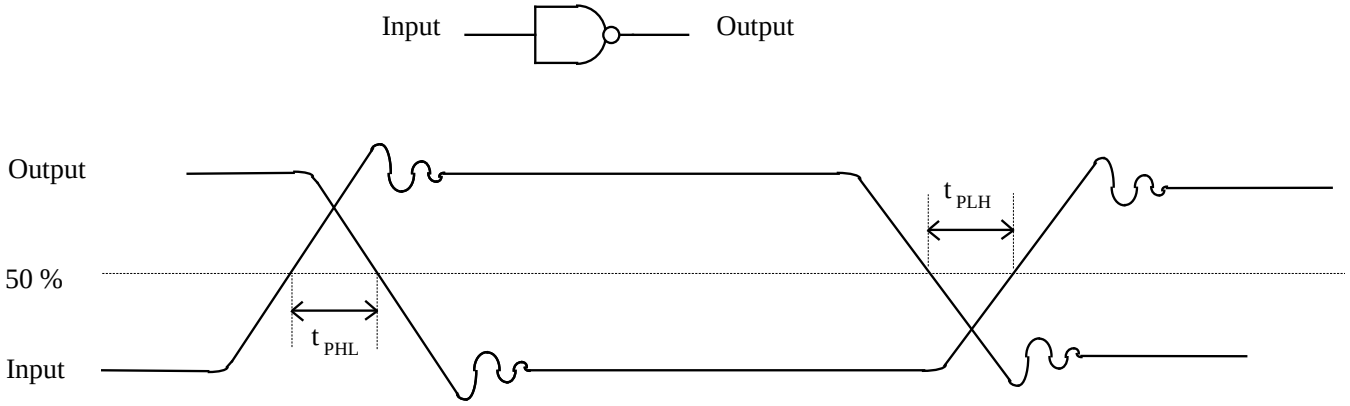


Figure 3: Propagation delay illustration

TTL logic circuits typically have one of two types of outputs:

- Totem-pole outputs
- Open-collector outputs

Totem-pole outputs

This is the most common type of output for TTL devices. Figure 1a below shows the internal circuitry of a 7400 2-input NAND. The transistors in TTL devices (denoted by Q) essentially act like switches. When a transistor is ON it acts like a closed switch and when a transistor is OFF it acts like an open switch. Note that transistor Q_4 is stacked on top of Q_3 like a totem-pole. The output Y is taken from the top of Q_3. Figure 1b shows the current path through the totem-pole when the output is HIGH and also when it is LOW.

When the output is HIGH: Q_4 is ON, Q_3 if OFF, and the current I_{OH} flows through Q_4 and out Y. Note that I_{OH} = 0.4 mA maximum.

When the output is LOW: Q_4 is OFF, Q_3 if ON, and the current I_{OL} flows in Y and through Q_3 to ground. Note that I_{OL} = 1.6 mA maximum.

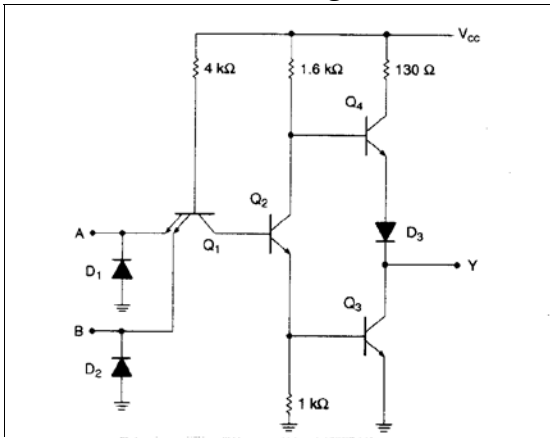


Figure 4A - 7400 NAND circuit

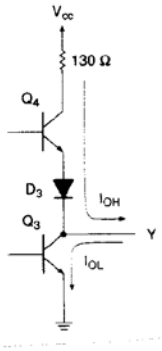


Figure 4B - current paths

Open-collector outputs

TTL circuits with open-collector outputs have only the lower transistor (Q_3) seen in the previous totem-pole output. Since there is no internal path from the output Y to the supply voltage V_{CC} , the circuit does not function properly unless an **external pull-up resistor** is used. . Figure 5a below shows the internal circuitry of a 7401 open-collector 2-input NAND. Figure 5b shows a 7401 NAND with an external pull-up resistor attached.

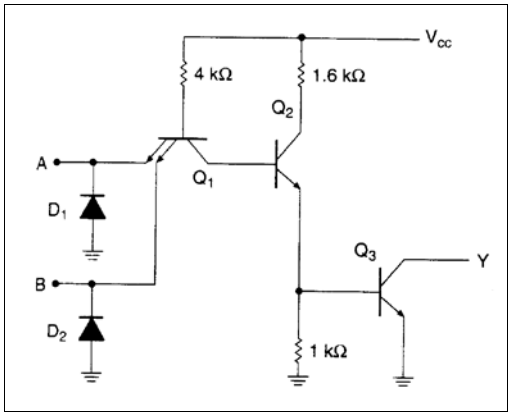


Figure 5a - 7401 open-collector NAND

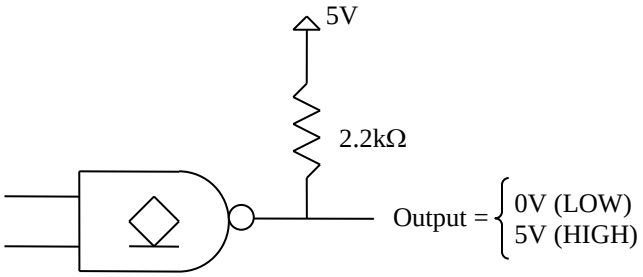


Figure 5b - 7401 NAND with pull-up resistor

Note that a special symbol is shown inside the NAND gate shown above. Open-collector gates are not always denoted with special symbols, but they may be indicated using one of the four symbols shown in Figure 6 below.

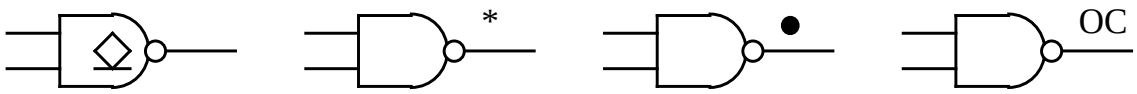


Figure 6 - Symbols for open-collector gates

Why should we use open-collector gates which require the addition of a pull-up resistor in order to function properly when we could use a gate with a totem-pole output instead? There are several reasons:

1) **Wired-ANDing** - Open-collector outputs can be tied directly together which results in the logical ANDing of the outputs. Thus the equivalent of an AND gate can be formed by simply connecting the outputs. This is especially convenient when large numbers of signals need to be ANDed. (Note that connecting the outputs of totem-pole gates will typically destroy them.)
2) **Increased current levels** - Standard TTL gates with totem-pole outputs can only provide a HIGH current output of 0.4 mA and a LOW current of 1.6 mA. Many open-collector gates have increased current ratings.
3) **Different voltage levels** - A wide variety of output HIGH voltages can be achieved using open-collector gates. This is useful in interfacing different logic families that have different voltage and current level requirements.

Providing different voltage levels with open-collector gates

Providing different HIGH voltage levels with open-collector gates is simply a matter of pulling the output up to the desired value using an external voltage source as illustrated in Figure 7 below.

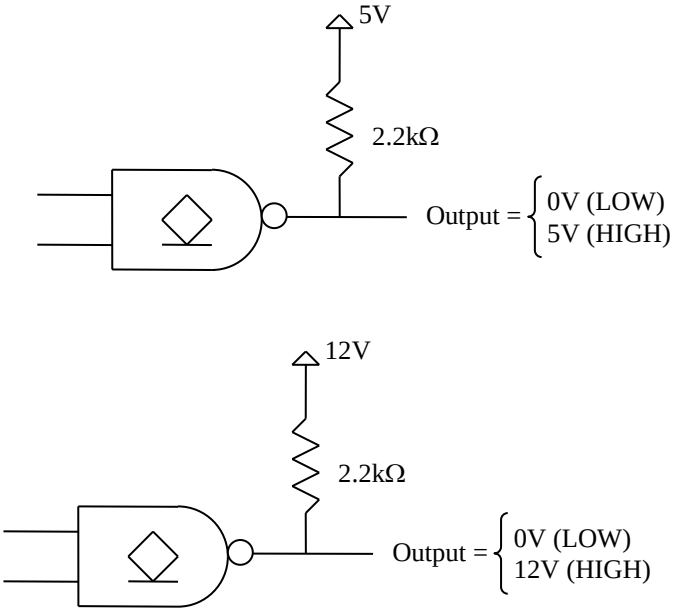
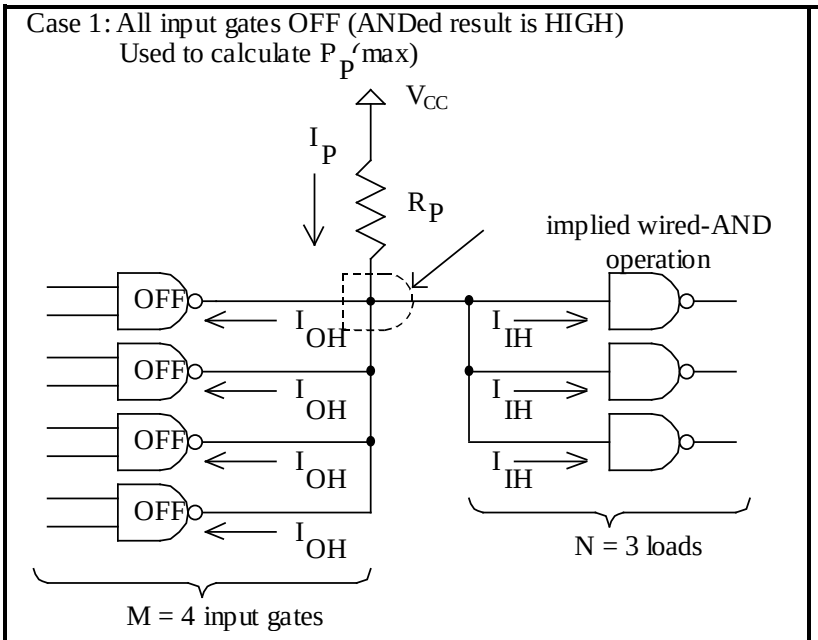


Figure 7: Open-collector gates with 5V and 12V outputs

Pull-up resistor calculation

Pull-up resistors are typically in the range of several hundred ohms to several thousand ohms, but exact ranges can be calculated using the relationships shown in Figures 8 and 9 below.



Calculation for R_P(max):

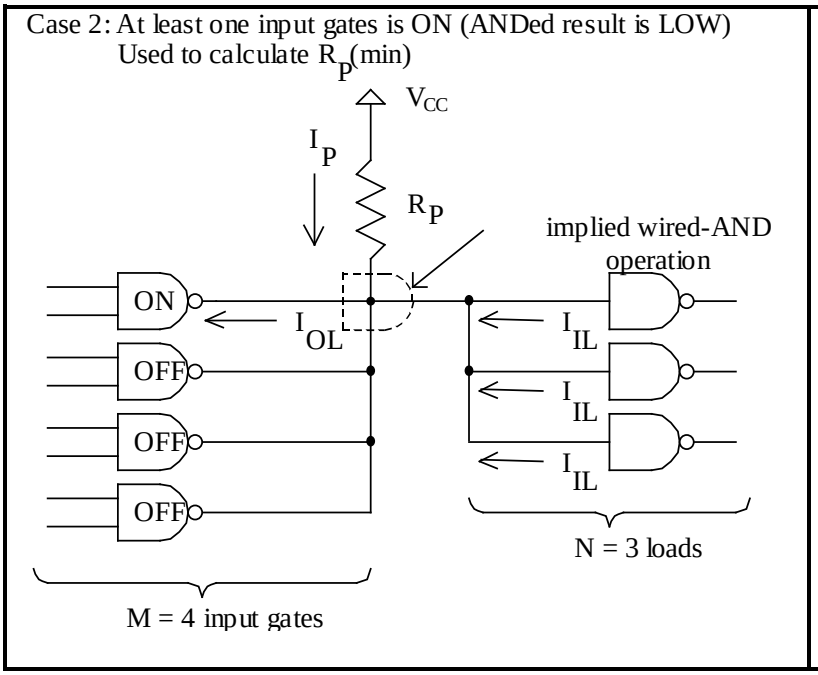
$$R_P(\max) = \frac{V_{CC} - V_{OH}(\min)}{M(I_{OH}) + N(I_{IH})}$$

Example: Using M = 4 and N = 3 as shown on the left and using standard TTL specifications:

$$R_P(\max) = \frac{5 - 2.4}{4(250\mu A) + 3(40\mu A)}$$

$$R_P(\max) = 2321\,\Omega$$

Figure 8 - Calculating the maximum pull-up resistor value



Calculation for R_P(min):

$$R_P(\min) = \frac{V_{CC} - V_{OL}(\max)}{I_{OL}(\max) + N(I_{IL})}$$

Example: Using M = 4 and N = 3 as shown on the left and using standard TTL specifications:

$$R_P(\min) = \frac{5 - 0.4}{16mA + 3(-1.6mA)}$$

$$R_P(\min) = 410\,\Omega$$

Figure 9 - Calculating the minimum pull-up resistor value

Open-collector drivers

Some open-collector gates are particularly well suited to driving loads that require higher voltage and current levels, such as incandescent lamps and relays. An example is the 7406 Hex Inverter Buffer/Driver. This gate is similar to the 7404 Hex Inverter (totem-pole output) except that I_{OL} (max) = 40 mA (instead of 16 mA) and V_{OH}(max) = 30 V (instead of around 5V). The term "driver" typically indicates that a device provides higher output currents.

An example is shown in Figure 10 below where the output of a 7406 is used to drive an incandescent lamp that requires a 12 V supply and about 35 mA of current. Note that a current-limiting resistor R_{limit} may or may not be necessary, depending on the resistance of the lamp filament.

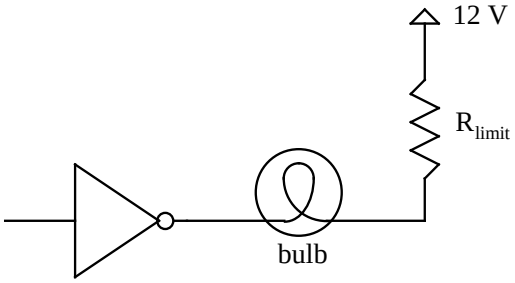


Figure 10 - 7406 driving an incandescent lamp

The 7406 allows us to drive loads that require up to 40 mA of current. For even larger currents, it may be necessary to use an output transistor. Transistors are available that can provide currents of several amperes. An example is shown in Figure 11 where a PNP power transistor is used to supply a current of 1A or more to a 12V DC motor.

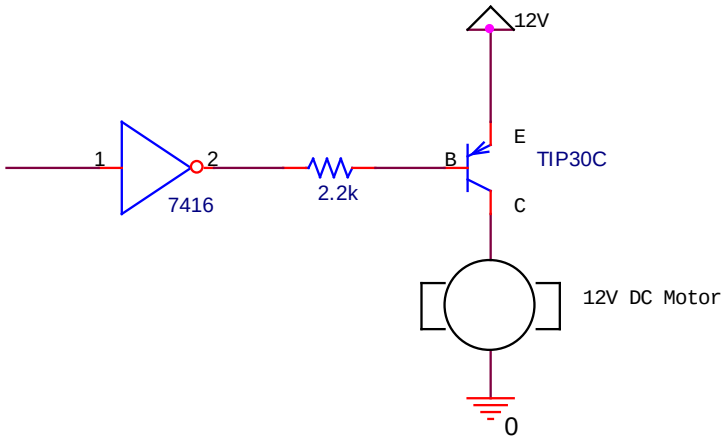


Figure 11 - Using an output transistor to provide large output currents

D. Preliminary Work

Include instructions with each step.

1. Calculate minimum and maximum values for pull-up resistors (R_P) under the following conditions. Use specifications for the 7401 (assume that $V_{OH}(min) = 2.4V$). Tabulate your results. Show a sample calculation for one case (both max and min value).

M (# inputs)	N (# outputs)	R_P(min)	R_P(max)	Are 1kΩ and 2.2kΩ between R_P(min) and R_P(max)?
1	0			
1	1			
1	3			
3	1			
3	3			

2. Refer to the data sheet for the 7400, 74LS00, and 74S00 and complete the table shown below. Include sample calculations for determining fanout, V_{NL}, and V_{NH}.

Specification	7400	74LS00	74S00
V_{CC}(min)			
V_{CC}(max)			
V_{IL}(max)			
V_{IH}(min)			
V_{OL}(max)			
V_{OH}(min)			
I_{IL}(max)			
I_{IH}(max)			
I_{OL}(max)			
I_{OH}(max)			
t_{PLH}(max)			
t_{PHL}(max)			
fanout (min)			
V_{NL}			
V_{NH}			

3. The 7404 is an inverter with totem-pole outputs. The 7406 and 7416 are inverters with open collector outputs. Refer to the data sheet for the 7404, 7406 and 7416. The TIP30C and TIP32C are pnp bipolar junction transistors (BJTs). You can locate data sheets online by visiting Jameco Electronics (www.jameco.com)

Specification	7404	7406	7416
V_{OH}(max)	5 V		
I_{OL}(max)			
I_{OH}(max)			

Specification	TIP30C	TIP32C	
V_{CE}(max) or V_{CEO}			(maximum collector-emitter voltage)
I_C(max)			(maximum DC collector current)

4. Include pinouts for the following ICs: 74LS00, 7401, 74LS06.

E. Laboratory Work

1. Measurement of Voltages and Currents

- Fill out the specified values in table shown below using the 74LS00 data sheet. Include the word MIN or MAX with each specification.
- Construct Circuit 1 using a 74LS00 IC. (Note that a NAND gate with its inputs tied together acts like an inverter.)
- Apply a HIGH input to the first gate (thus the output is LOW) and measure the input current (I_{IL}) to the second gate and the output voltage (V_{OL}) of the first gate using a digital multimeter.
- Repeat the measurements with a LOW input to the first gate (thus the output is HIGH) and measure the input current (I_{IH}) to the second gate and the output voltage (V_{OH}) of the first gate.
- Record the results in the table below and verify that these values are within specified limits.

	Measured Value	Specified Value	Within Specs?
I_{IL}			
V_{OL}			
I_{IH}			
V_{OH}			

- Ask the instructor to look at the results above to be sure that they look correct.

2. Logic Probes

Connecting the logic probe to HIGH or LOW points on a circuit will result in different colored LEDs lighting and different sounds from the probe.

- Practice using a logic probe on Circuit 1 by checking a HIGH voltage (on pin 14) and a LOW voltage (on pin 7). Record the lights lit and sounds made in the table below.

Use Logic Probe to measure	Color LED lit	Sound made (high pitch or low pitch)
HIGH Voltage (pin 14)		
LOW voltage (pin 7)		

- Next use a logic probe to check the inputs and outputs on an unused gate on the 74LS00 (no wires connected to the input or output, but powered up). Complete the table below.

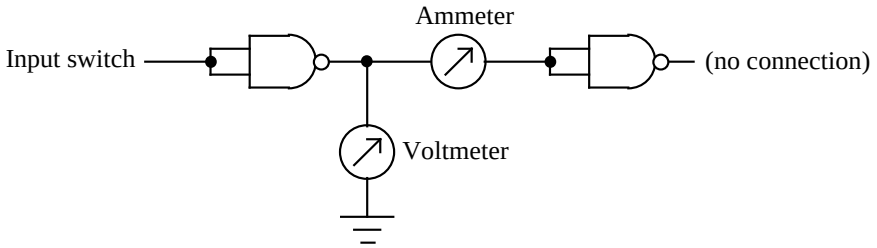
Use Logic Probe to measure	Results (LOW, HIGH, or NO READING)
Open inputs	
Open output	

- Record the truth table for a 74LS00 NAND below.

A	B	$\overline{A \cdot B}$
0	0	
0	1	
1	0	
1	1	

- Include the truth table in your report. Highlight the line in the truth table that illustrates the only case where the output of the NAND is LOW.
- Based on the truth table above and your results using a logic probe on an unused gate, complete the following statement:

> Since the open output of the 74LS00 read _____, it can be stated that "OPEN INPUTS FOR 7400 SERIES GATES ACT LIKE _____ ."



Circuit 1

3. **Propagation Delay Measurement** (Note: The instructor may set up this step as a demonstration. If so, be sure to get a printout of the waveforms showing t_{PHL} and t_{PLH}. Clearly label t_{PHL} and t_{PLH} exactly where they are measured on the printouts and label the input and the output.

- Measure t_{PLH}: Construct Circuit 2 shown below using the function generator and oscilloscope settings indicated below. Turn on the oscilloscope before turning on the computer and then run program **WaveStar for Oscilloscopes**. View both waveforms A and B on the oscilloscope and adjust the time scale until you can see t_{PLH} . Add two time cursors at the 50% points on waveforms and the difference between the cursors (also displayed) will be t_{PLH}. Capture the image with WaveStar and print it or cut and paste the images to Word. Clearly label (by hand) where t_{PLH} is measured on the printed waveform. Also label the input and the output on the printout. Include the printout in your report.
- Repeat the step above to measure t_{PHL} .
- Compare the measured values to values found in the spec. sheet (see table below).
- Ask the instructor to look at the your results to be sure that they look correct.

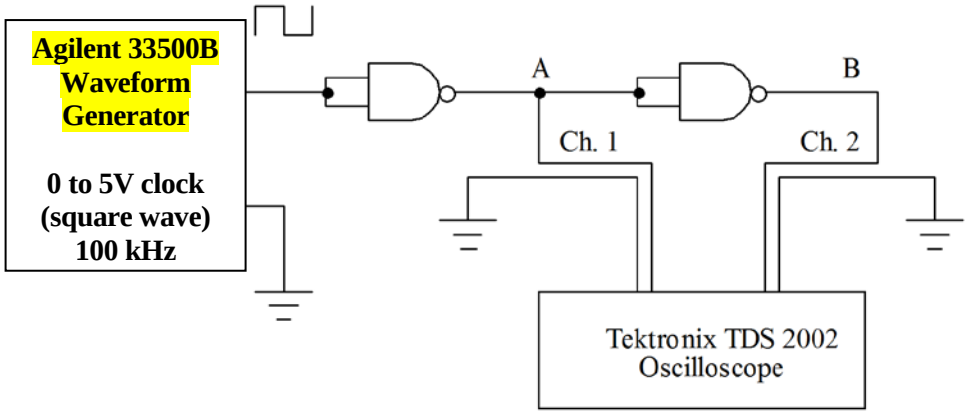
Use the following settings for the function generator and the oscilloscope. (Note: Pressing ***AUTO SET*** on the oscilloscope will typically result in the correct settings!)

Tektronix TDS 2002 Oscilloscope

Control	Setting
Ch. 1/Ch. 2 Menu	*Coupling: DC* *BW limit: OFF* *V/div: Coarse* *Probe: 1X* *Invert: Off*
Trigger Menu	Type: Edge Source: Ch. 1 Slope: Rising Mode: Auto Coupling: DC
Ch.1 V/div	1V
Ch. 2 V/div	1V

Agilent 33500B Waveform Generator

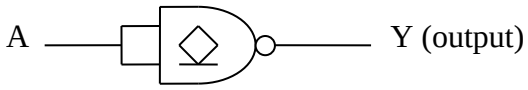
Control	Setting
Waveform	⊓⊔ (square wave)
Frequency *	100 kHz
Amplitude *	5 Vpp
Offset *	2.5 V
* Enter the value and then a choice of units will be shown using the buttons under the screen).	



Circuit 2: Measurement of t_{PHL} and t_{PLH}

	Measured Value	Specified Value	Within Specs?
t_{pHL}			
t_{pLH}			

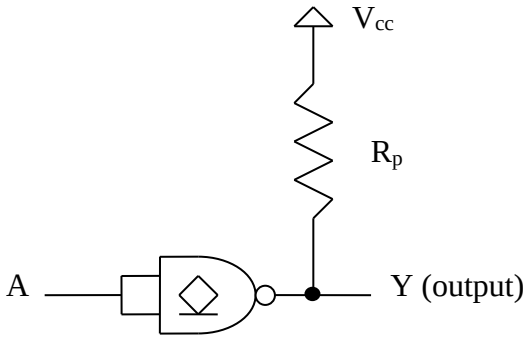
4. **Open-collector gate without a pull-up resistor**
   - Connect a 7401 open-collector NAND with its inputs tied together (to act as an inverter) with no load and no pull-up resistor as shown in Circuit 3.
   - Measure the output with a voltmeter for both HIGH and LOW inputs.
   - Are both of the output voltages within specified ranges? (One should be out of specs.) Assume that $V_{OH}(min) = 2.4V$.
   - Ask the instructor to look at the your results to be sure that they look correct.



Circuit 3

Input Switch A	Output Logic Level	Output Voltage	Specified Voltage	Within specs?
L	H			
H	L			

5. **Open-collector gate with a pull-up resistor**
   - Connect a 7401 open-collector NAND with its inputs tied together (to act as an inverter) and with no load using a pull-up resistor as shown in Circuit 4. Use $V_{cc} = 5V$.
   - Use a pull-up resistor that is within the range calculated in the Preliminary Work.
   - Measure the output with a voltmeter for both HIGH and LOW inputs.
   - Are both of the output voltages within specified ranges? (They should be.) Assume that $V_{OH}(min) = 2.4V$.
   - Ask the instructor to look at the your results to be sure that they look correct.



Circuit 4

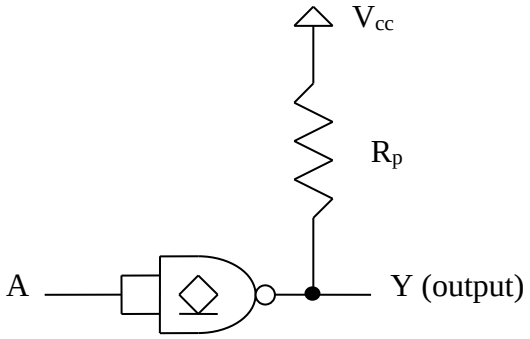
Input Switch A	Output Logic Level	Output Voltage	Specified Voltage	Within specs?
L	H			
H	L			

- Record the value of R_P used in the circuit above and compare it to $R_{P(min)}$ and $R_{P(max)}$ calculated in the Preliminary Work.

$R_{P(min)}$	
$R_{P(max)}$	
R_P : value used in Circuit 4 above	

6. **Open-collector gate with a pull-up resistor**

- Note that two channels of the DC power supply are needed in this step (5V and 12V).
- Modify Circuit 4 used in the last step such that the pull-up resistsor is connected to a 12V supply. **Warning: Connect the pull-up resistor to 12V, but be sure to power the 7401 using only 5V.**
- Measure the output with a voltmeter for both HIGH and LOW inputs.
- Are the results as expected?
- Ask the instructor to look at the your results to be sure that they look correct.



Circuit 4

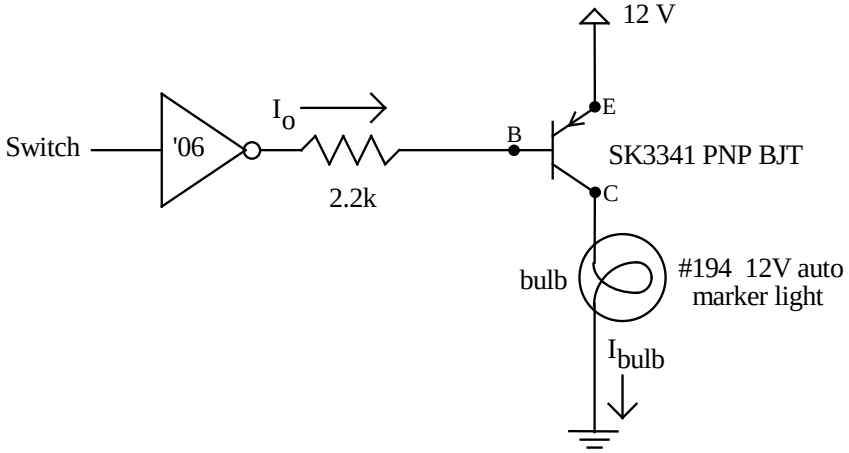
Input Switch A	Output Logic Level	Output Voltage
L	H	
H	L	

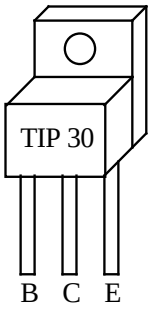
7. **Driving an incandescent lamp using an output transistor**

- Connect Circuit 5 using either a 74LS06 or 7416 open-collector inverter. Use an SK3341, TIP30, TIP 32 or equivalent PNP power transistor (not a TIP 31). **Warning: Connect 12V to the transistor, but be sure to power the 7406 using only 5V.**
- For both input switch positions, measure and record the 7406 current and voltage as well as the current through the bulb.

Input Switch A	Output Logic Level	V_o (7406)	I_o (7406)	I_{bulb}	Bulb lit?
L	H				
H	L				

- Ask the instructor to look at the your results to be sure that they look correct.





TIP 30 Pin Assignment

Circuit 5

8. **Driving a 12V DC motor using an output transistor**
   - Replace the bulB in Circuit 5 with a 12V DC motor and repeat the measurements.

Input Switch A	Output Logic Level	V_o (7406)	I_o (7406)	I_{motor}	Motor running?
L	H				
H	L				

   - Ask the instructor to look at the your results to be sure that they look correct.

Report

Remember that each lab report should have the following four sections. See additional notes below.

Title Page

Preliminary Work

- Include instructions

Lab Results

- Include all measured results. Use tables to summarize results whenever possible. (Do not simply fill in the sheet from the lab guide. This is not acceptable.)
- Include step numbers and titles or headings that make it clear what is being shown.
- Include units whenever appropriate.

Discussion/Conclusion

- Discuss each part of the experiment performed in lab.
- Are the results as expected? Were all results withing specifications? If any results were not within specifications, discuss possible reasons.
- What have you proven or demonstrated by completing each step of the experiment?
- Explain any errors.
- Discuss in general when it would be appropriate to use totem-pole gates, open-collector gates, and/or transistors.