EGR 270 Due date: See Due Dates Table
Fundamentals of Computer Engineering
File: N270H5

Homework Assignment #5

Reading Assignment:

Chapter 3 in the textbook Logic and Computer Design Fundamentals, 5th Edition by Mano

Problem Assignment:

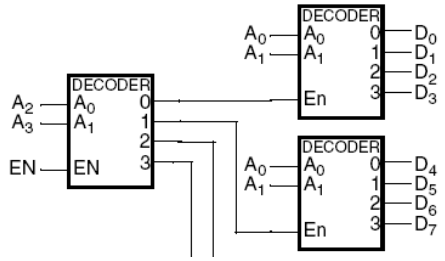
1) Chapter 3 problems: 29, 35, 36, 37, 40, 44, 46, 48
   Correction: In problem 3-36 there are inputs I0 - I9, not I1 – I9.
2) A combinational logic circuit has 3 outputs as described below:

$$F_1 = \Sigma(0,3,4) \quad F_2 = \Sigma(1,2,7) \quad F_3 = \Pi(0,1,2,4)$$

   A) Implement the circuit using a single decoder with active-HIGH outputs and external 2-input OR gates
   B) Implement the circuit using a single decoder with active-LOW outputs and external 2-input AND gates
3) See worksheet on page 3.

Selected Answers:

3-29) (partial diagram)

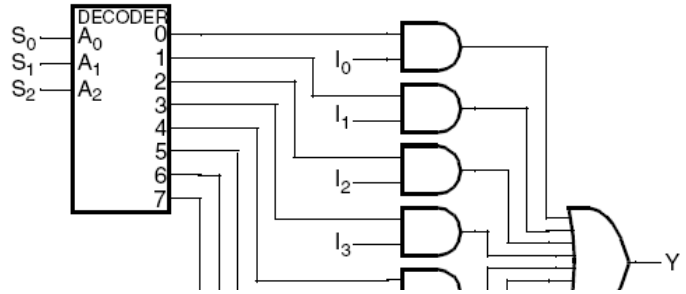


3-36) (partial truth table)

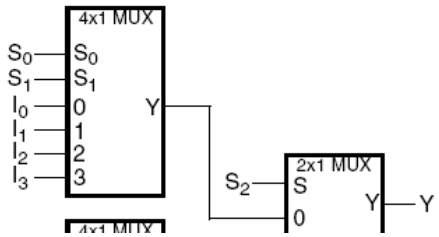
Decimal Inputs										Binary Outputs				
9	8	7	6	5	4	3	2	1	0	A_3	A_2	A_1	A_0	V
0	0	0	0	0	0	0	0	0	0	X	X	X	X	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	1	X	0	0	0	1	1

3-37) (partial diagram)

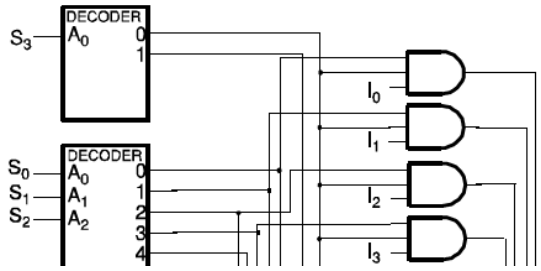
a)



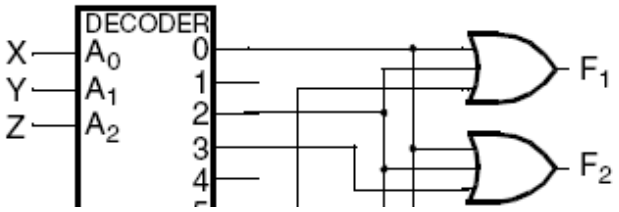
b)



3-40) (partial diagram)

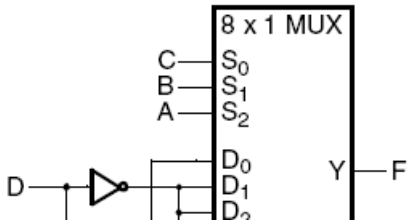


3-44) (partial diagram)

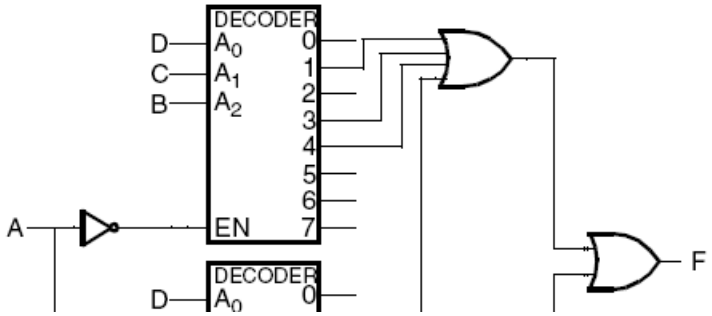


3-46) (partial mux table and diagram)

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	0	$F = 0$
0	0	1	0	1	
0	0	1	1	0	$F = \overline{D}$



3-48) (partial diagram)

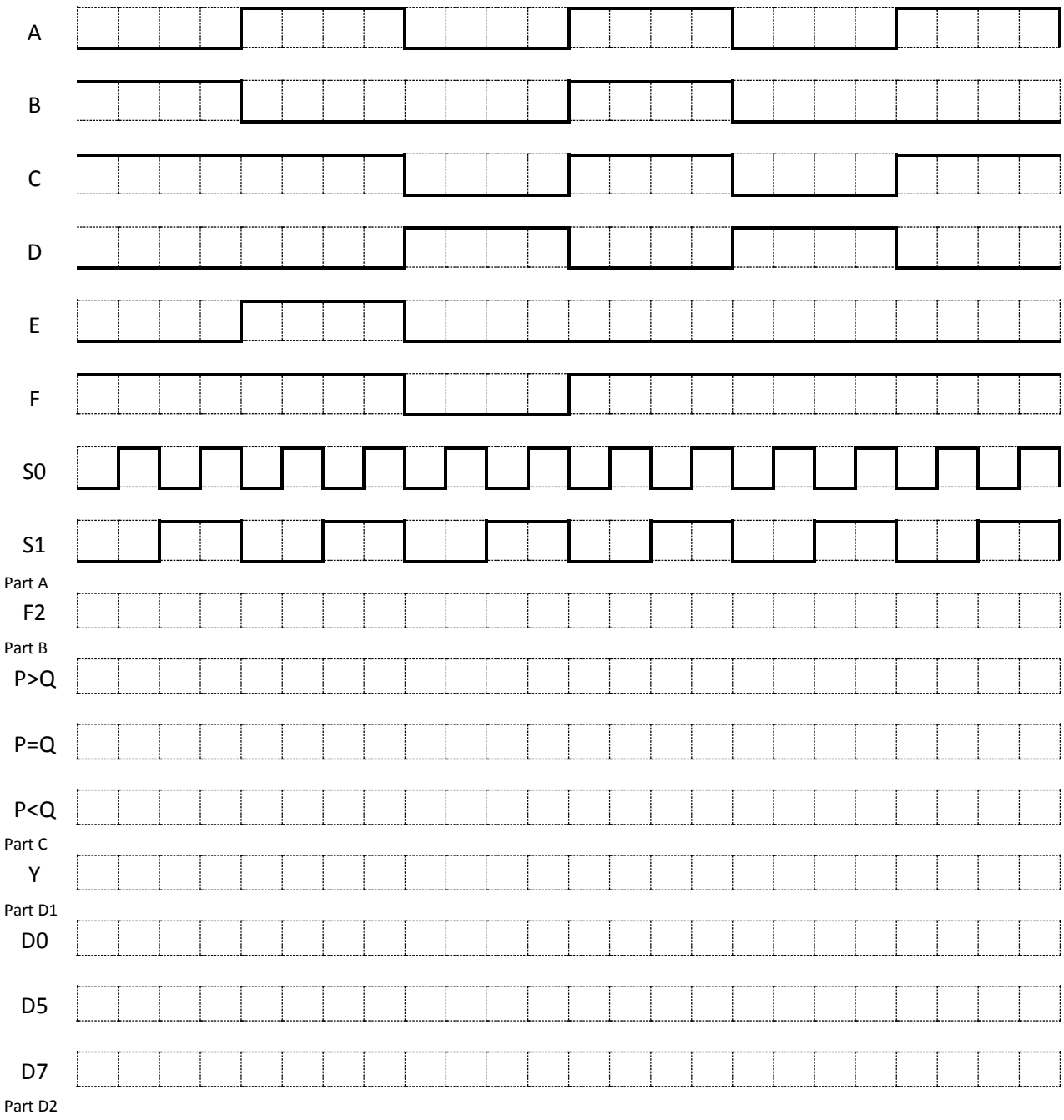


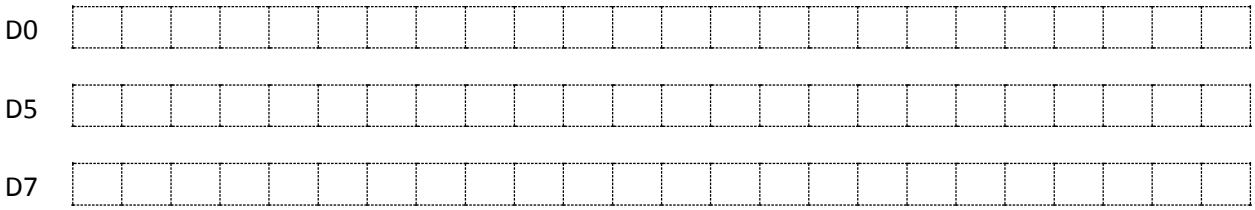
2A) To generate F1, OR decoder outputs D0, D3, and D4. Similar approach for F2 and F3.
2B) To generate F1, AND decoder outputs D1, D2, D5, D6, and D7

Name: _____

EGR 270 HW #5 (continued) – ***Turn in this worksheet as part of the assignment***

3) Timing Diagrams: Using the input waveforms below, sketch the outputs described in each part below.
   A. Sketch the output $F_2 = AB + AC + BC$ using the input waveforms A, B, and C shown below.
   B. If a 3-bit magnitude comparator has inputs P = ABC and Q = DEF (A and D are the MSBs) using the waveforms A-F below, sketch the 3 outputs of the comparator (P>Q, P=Q, P<Q).
   C. If A, B, C, and D are the input lines to a 4 x 1 multiplexer (A = input 0), and S1, S0 are the select lines, sketch the output Y.
   D. If A, B, and C are the inputs to a 3-line-to-8-line decoder, sketch the outputs D0, D5, and D7 if:
      1) waveform E is an active LOW enable and the outputs are active LOW
      2) waveform F is an active HIGH enable and the outputs are active HIGH




D0
D5
D7