EGR 270 Due date: See Due Dates Table
Fundamentals of Computer Engineering
File: N270H3

Homework Assignment #3 – Karnaugh Maps

Reading Assignment:

Chapter 2 in the textbook Logic and Computer Design Fundamentals, 5th Edition by Mano

Problem Assignment:

1) (75 pts) Chapter 2 problems (part a & b only for all problems): 14, 15, 17, 18, 19, 22, 23, 24, 26
2) (6 pts) Determine minimal SOP expressions for each part below using 5-variable Karnaugh maps
   a. F(A,B,C,D,E) = Σm(0,1,4,5,16,17,21,25,29)
   b. F(A,B,C,D,E) = A'B'CE' + A'B'C'D' + B'D'E' + B'CD' + CDE' + BDE'
3) (6 pts) Minimize each of the following expressions using K-Maps (make use of XOR gates if they reduce the number of gates):
   a) f(A,B,C) = Σ (1,3,4,6)
   b) f(A,B,C,D) = Σ(0,2,5,7,8,10,13,15)
   c) f(A,B,C,D) = Σ (0,3,5,6,9,10,12,15)
4) (4 pts) Determine the gate input cost for the original expression and for the minimized result for problem 2-15 (parts A & B only).

Problem	Gate Input Cost (original circuit)	Gate Input Cost (original circuit)
2-15a		
2-15b		

5) (9 pts) A circuit output is described by F = A(BC' + CD') + B'(AC + D(A'+C')).
   a) Use a K-map to find a minimal SOP expression for F.
   b) Use a K-map to find a minimal POS expression for F.
   c) Complete the table below. Include inverters and assume that logic gates are available with any number of inputs.

	Original expression	Minimal SOP	Minimal POS
Number of gates			
Number of literals			
Gate input cost			
Number of gate delays			

Problem Format and Solutions: (See notes on Homework #1)

Selected Answers:

2.14) a) X'Y + YZ + XY'Z'
2.17) a) F = X'Z' + Y'Z' + W'X'Y' + W'XYZ
2.23) a) SOP: ABC' + A'BD + A'B'C or SOP: AC'D' + BC'D + A'CD + B'CD'
POS: (A'+B+D')(A'+B'+C')(A+B'+D)(A+B+C) or
POS: (A+C+D)(B+C+D')(A'+C'+D')(B'+C'+D)
2.24) a) F = A + C'

2.26) a) SOP: 5 possible minimal solutions:
SOP: F = WY + YZ' + W'Y'Z + WXZ' or
SOP: F = (X'Y' or X'Z) + W'YZ + W'Y'Z' + (WXZ or WY'Z)
POS: 4 possible minimal solutions:
POS: F = ((X+Y) or (X+Z))(W+Y'+Z')(W+Y+Z)((W'+X'+Z') or (W'+Y+Z'))

2a) F(A,B,C,D,E) = A'B'D' + AD'E + B'C'D'

2b) F(A,B,C,D,E) = A'B'D' + B'D'E' + B'CD' + CDE' + BDE'

3) a) $A \oplus C$ b) $\overline{B} \oplus D$ c) $\overline{(B \oplus D) \oplus (A \oplus C)}$

4) Partial solution:

Problem	Gate Input Cost (original circuit)	Gate Input Cost (minimized circuit)
2-15a	12	8
2-15b		

5) Partial solution:

	Original expression	Minimal SOP	Minimal POS
Number of gates	14		
Number of literals			10
Gate input cost		14	
Number of gate delays			3