EGR 270 Lab Information

Lab Policies

- The lab grade makes up 25% of the course grade for EGR 270.
- Each lab session will begin with a lecture by the instructor on the following lab. Attendance for the lectures is critical as new material is introduced in many of the labs.
- Students may work alone or with a partner one some of the labs. However, some labs require the design and/or implementation of customized circuits (on the EmplID, for example), so students must work alone on these labs.
- Each student must submit their own lab report for each lab.
- Lab reports are due on the date of the next lab. For example, Lab Report #2 is due on the day the the class will be performing Lab #3.
- The key to each lab is proper verification of circuit operation. Therefore,
    - If you do not complete a lab during the class session, you can use the lab during open lab times and let the instructor know when you are ready to demonstrate each circuit.
    - If you miss a class (not advised), you can demonstrate each circuit whenever the instructor is available. Note that the instructor should be notified if a lab is to be missed so that other arrangements can be made.
    - If you would like to work ahead and reduce the amount of time spent in lab, you can work in the lab (or check out a breadboard and components) and demonstrate each circuit whenever the instructor is available.

Lab Grading

- The lab grade makes up 25% of the course grade for EGR 270.
- All labs require verification of proper circuit operation by the instructor.
- Lab reports will not be accepted until all circuits in the lab have been built and verified.
- The grade for the lab portion of EGR 270 is simply the average of the lab report grades.
- All labs require that a Preliminary Work section be completed before lab. The Preliminary Work will be briefly checked by the instructor and will affect the lab report grade as follows:
    - Preliminary Work completely done – full credit on lab report
    - No Preliminary Work done: deduct 10 points from lab report grade
    - Preliminary Work partially done: deduct 1 to 9 points from lab report
- Note that the Preliminary Work will also be graded for accuracy and completeness when it is submitted as part of the lab report.

(continued)

Tentative Schedule

Date	Topic
Jan 8	No class
Jan 15	Introduction to lab equipment, course procedures, etc.
Jan 22	Lab #1: Introduction to Logic Circuits
Jan 29	Lab #2: Characteristics of TTL gates
Feb 5	Test 1 or Lab #2 continued (if necessary)
Feb 12	Test 1 or Lab #2 continued (if necessary)
Feb 19	Lab #3: Combinational Logic Circuits
Feb 26	Lab #4: 7-segment displays, decoders, and multiplexers
Mar 4	Lab #5 VHDL Combinational Logic Circuit
Mar 11	TCC Closed – Spring Break
Mar 18	Test 2 or Lab #5 continued (if necessary)
Mar 25	Test 2 or Lab #5 continued (if necessary)
Apr 1	Lab #6: Sequential Counters
Apr 8	Lab #7: VHDL Sequential Logic Circuit
Apr 15	Lab #8: Assembly language/MicroStamp11
Apr 22	Lab #8 continued (if necessary)