

- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Functionally Interchangeable With the Signetics NE555, SA555, SE555, SE555C; Have Same Pinout**

**SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS**

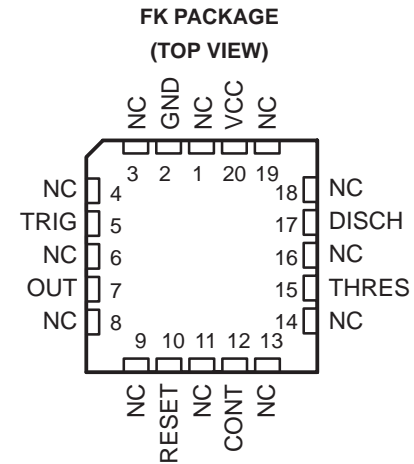
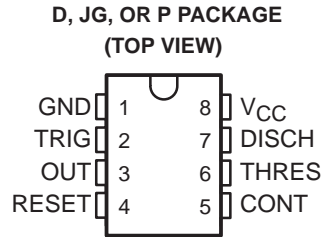
### description

These devices are precision monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of  $V_{CC}$ . These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. RESET can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between DISCH and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The NE555 is characterized for operation from 0°C to 70°C. The SA555 is characterized for operation from –40°C to 85°C. The SE555 and SE555C are characterized for operation over the full military range of –55°C to 125°C.



NC—No internal connection

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE					CHIP FORM (Y)
	V <sub>THRES</sub> max V <sub>CC</sub> = 15 V	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)	
0°C to 70°C	11.2 V	NE555D			NE555P	NE555Y
–40°C to 85°C	11.2 V	SA555D			SA555P	
–55°C to 125°C	10.6 V	SE555D	SE555FK	SE555JG	SE555P	
	11.2 V	SE555CD	SE555CFK	SE555CJG	SE555CP	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

# NE555, NE555Y, SA555, SE555, SE555C PRECISION TIMERS

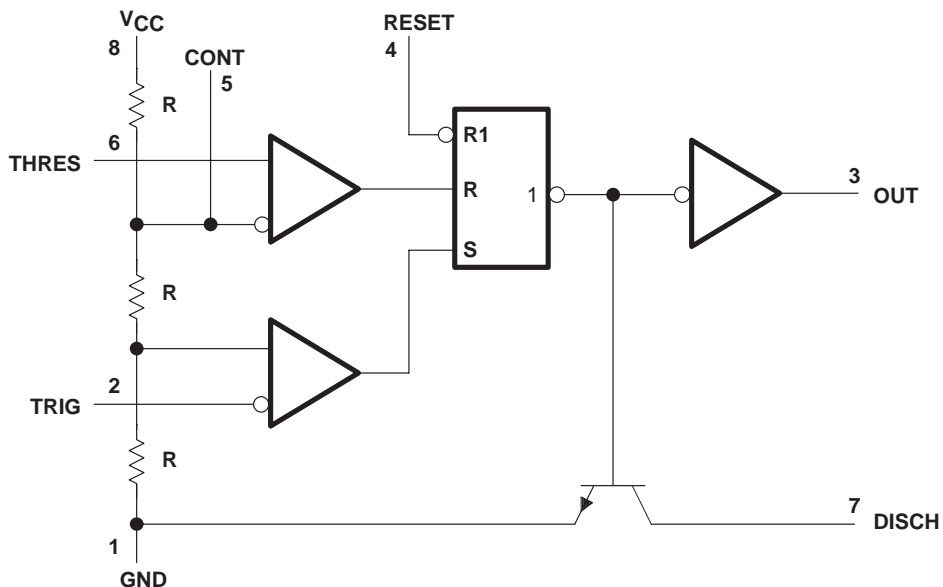
SLFS022 – SEPTEMBER 1973 – REVISED FEBRUARY 1992

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V <sub>DD</sub>	Irrelevant	High	Off
High	> 1/3 V <sub>DD</sub>	> 2/3 V <sub>DD</sub>	Low	On
High	> 1/3 V <sub>DD</sub>	< 2/3 V <sub>DD</sub>	As previously established	

† Voltage levels shown are nominal.

## functional block diagram

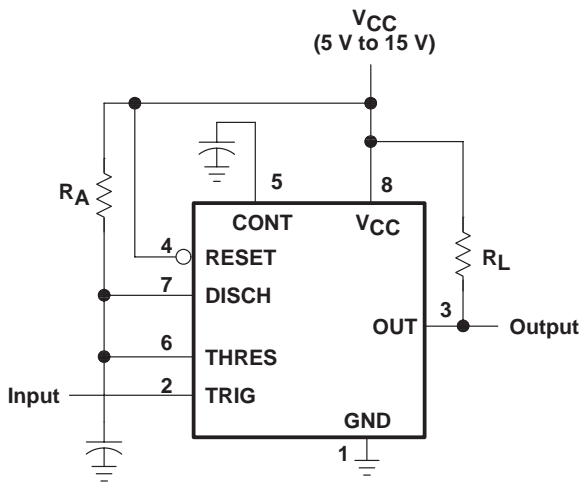


RESET can override TRIG, which can override THRES.  
Pin numbers shown are for the D, JG, and P packages only.

APPLICATION INFORMATION

monostable operation

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to TRIG sets the flip-flop ( $\bar{Q}$  goes low), drives the output high, and turns off Q1. Capacitor C is then charged through  $R_A$  until the voltage across the capacitor reaches the threshold voltage of THRES input. If TRIG has returned to a high level, the output of the threshold comparator will reset the flip-flop ( $\bar{Q}$  goes high), drive the output low, and discharge C through Q1.



Pin numbers shown are for the D, JG, and P packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately  $t_w = 1.1R_A C$ . Figure 11 is a plot of the time constant for various values of  $R_A$  and C. The threshold levels and charge rates are both directly proportional to the supply voltage,  $V_{CC}$ . The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to  $V_{CC}$ .

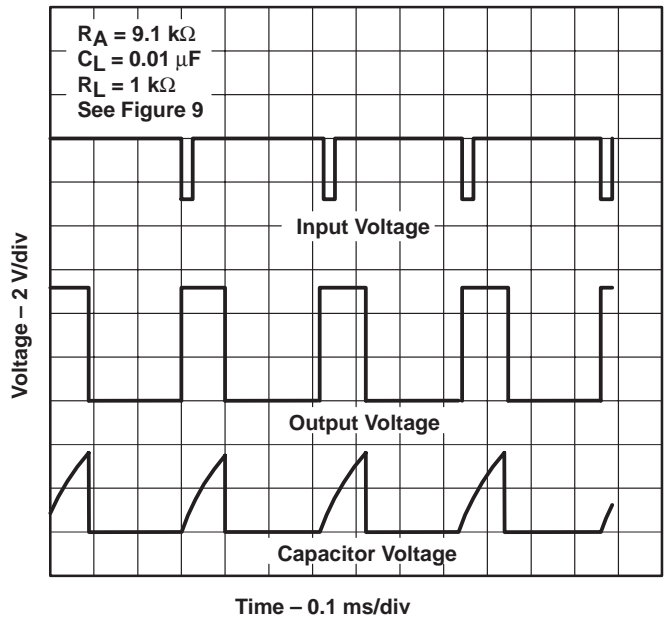


Figure 10. Typical Monostable Waveforms

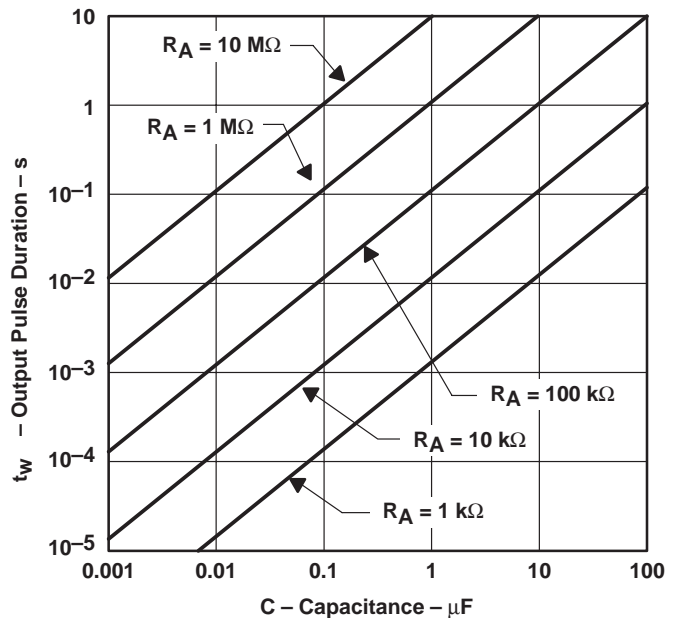


Figure 11. Output Pulse Duration vs Capacitance

# NE555, NE555Y, SA555, SE555, SE555C PRECISION TIMERS

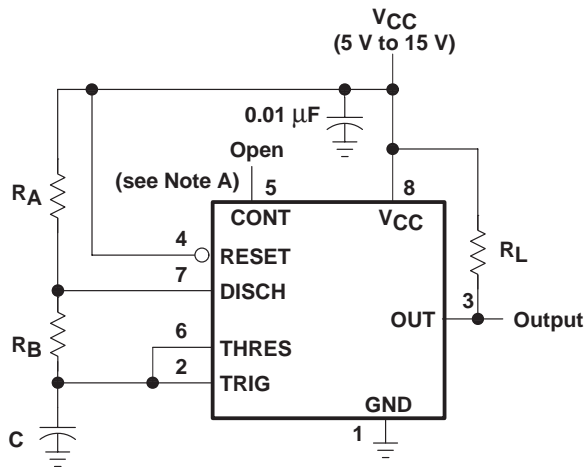
SLFS022 – SEPTEMBER 1973 – REVISED FEBRUARY 1992

## APPLICATION INFORMATION

### astable operation

As shown in Figure 12, adding a second resistor,  $R_B$ , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor  $C$  will charge through  $R_A$  and  $R_B$  and then discharge through  $R_B$  only. The duty cycle may be controlled, therefore, by the values of  $R_A$  and  $R_B$ .

This astable connection results in capacitor  $C$  charging and discharging between the threshold-voltage level ( $\approx 0.67 \cdot V_{CC}$ ) and the trigger-voltage level ( $\approx 0.33 \cdot V_{CC}$ ). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.



Pin numbrs shown are for the D, JG, and P packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor may improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

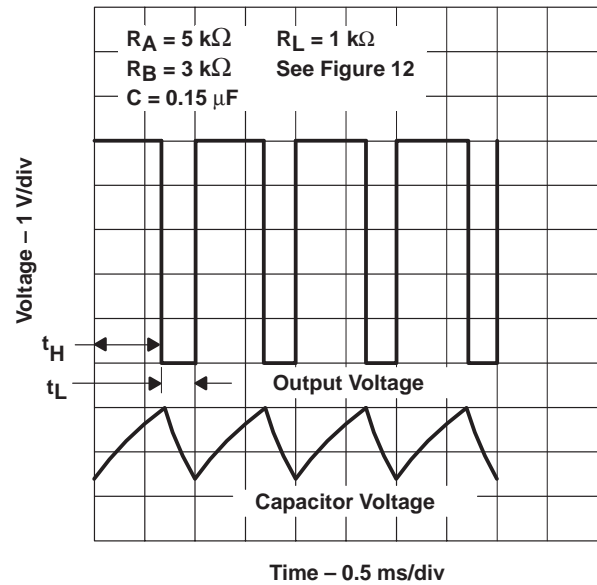


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration  $t_H$  and low-level duration  $t_L$  may be calculated as follows:

$$t_H = 0.693 (R_A + R_B) C$$

$$t_L = 0.693 (R_B) C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693 (R_A + 2R_B) C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B) C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

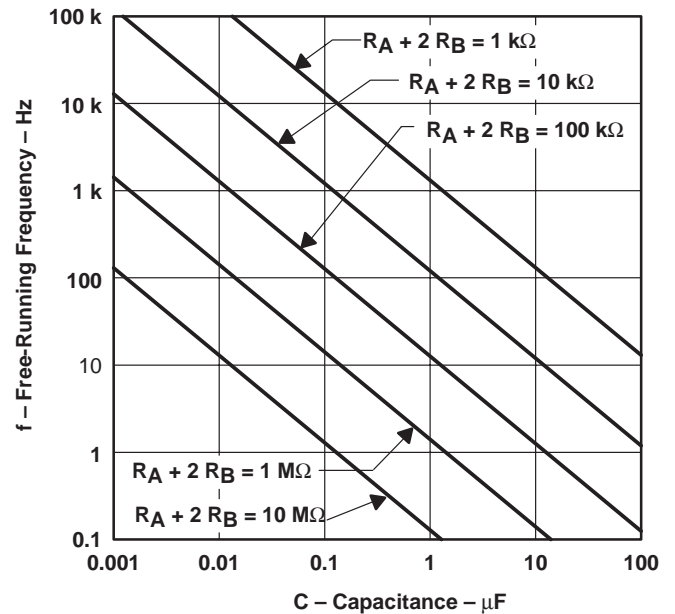
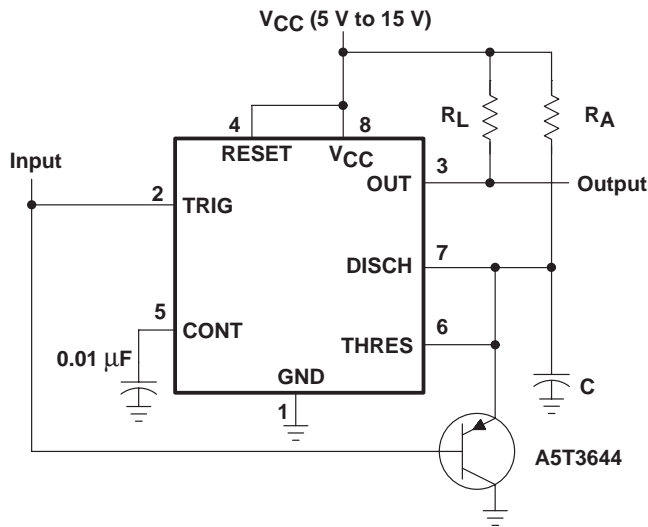


Figure 14. Free-Running Frequency

missing-pulse detector

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.



Pin numbers shown are shown for the D, JG, and P packages.

Figure 15. Circuit for Missing Pulse Detector

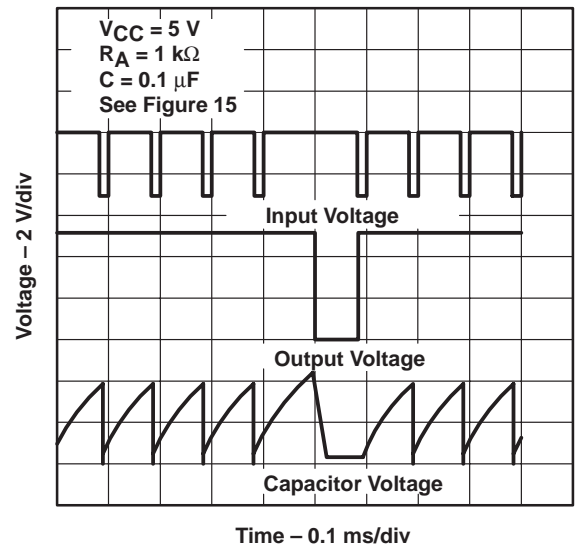


Figure 16. Circuit for Missing Pulse Detector

## APPLICATION INFORMATION

### frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

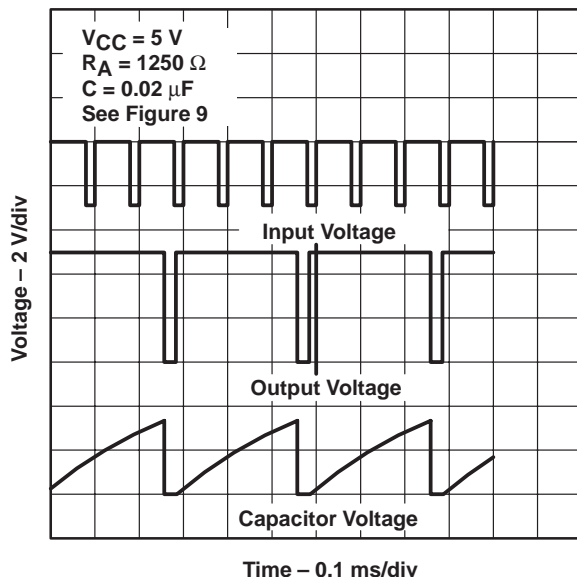
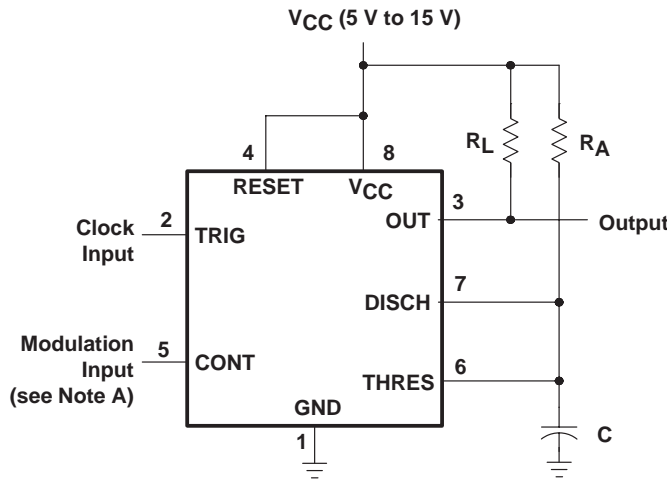


Figure 17. Divide-By-Three Circuit Waveforms

### pulse-width modulation

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, and P packages only.

NOTE A: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

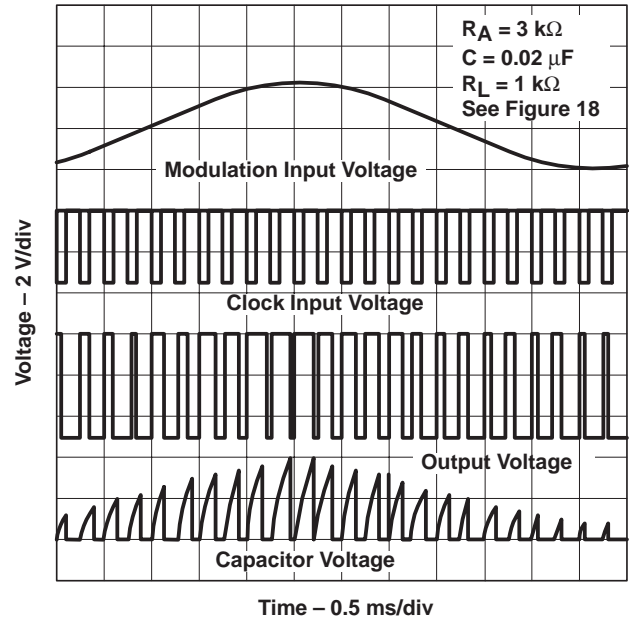
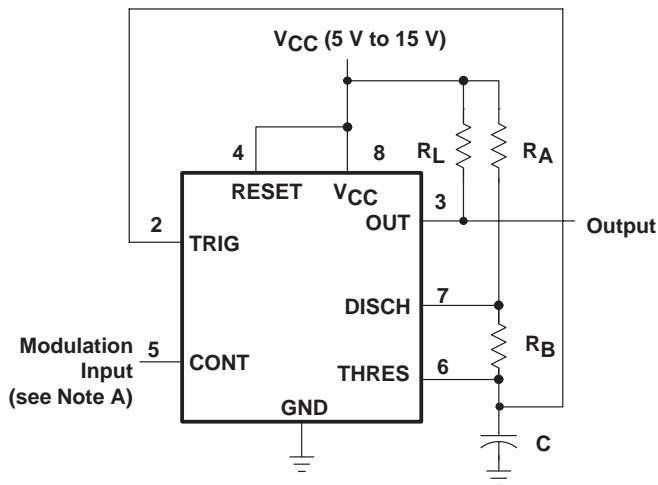


Figure 19. Pulse-Width Modulation Waveforms

pulse-position modulation

As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrates a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, and P packages only.

NOTE A: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

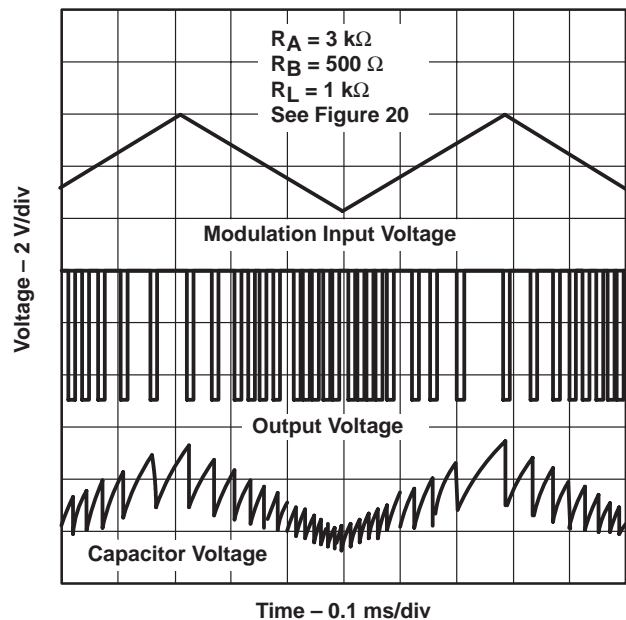
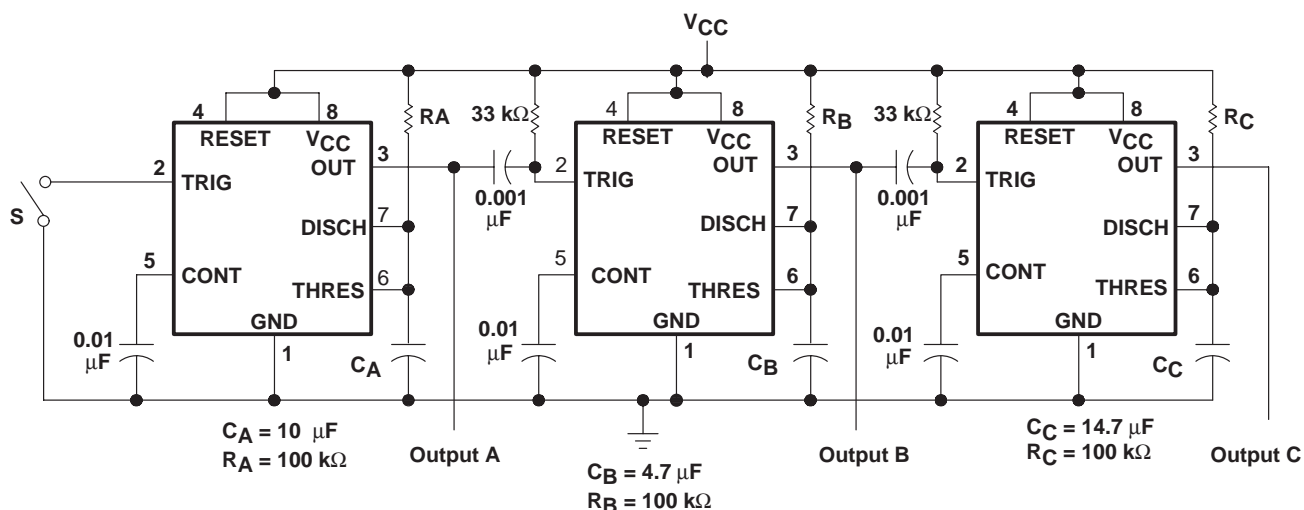


Figure 21. Pulse-Position-Modulation Waveforms

## APPLICATION INFORMATION

### sequential timer

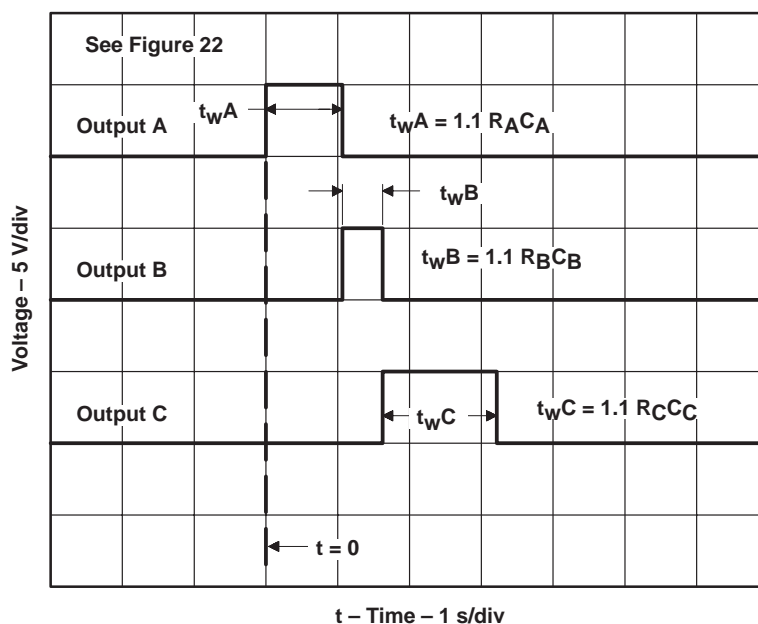


S closes momentarily at  $t = 0$ .

Pin numbers shown are for the D, JG, and P packages only.

**Figure 22. Sequential Timer Circuit**

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



**Figure 23. Sequential Timer Waveforms**